Evaluation of Energy-Recovering Interconnects for Low-Power 3D Stacked ICs

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***Abstract*—Energy-recovering schemes have been proposed in the literature as an alternative approach to low-power design, while their performance has been demonstrated to be extremely promising when driving large capacitive loads, such as clock distribution networks [1]. This work investigates the potential of the energy-recovering methodology for improving the energy efficiency of through-silicon via (TSV) interconnects in 3D ICs.**

I. Introduction

Energy dissipation is a major concern for battery-powered mobile systems. In 3D stacked ICs, TSV interconnects enable low-parasitic direct connections between tiers and can allow for considerable energy savings when compared to traditional PCB chip-to-chip interconnections [2]. However, TSV parasitic capacitance can still become an important source of energy dissipation in large, densely interconnected 3D SoCs, since the combined capacitance and thus the energy required to drive TSVs, will increase linearly with the number of tiers and interconnections.

Energy-recovering logic has demonstrated great potential when driving large capacitive loads and circuits utilizing this technique have been successfully implemented in the past [1], [5]. Energy-recovering designs can break the $C \cdot V_{DD}$ energy limit of conventional static CMOS, by spreading out charge transfer more evenly over an entire switching period and thus making energy dissipation proportional to the operating frequency [3]. The result is very low energy dissipation which can asymptotically approach zero at low operating frequencies [4].

In this paper, an energy-recovering configuration for 3D ICs is presented and an analysis is attempted based on theoretical models. The proposed circuit is evaluated against conventional static CMOS, while the energy efficiency dependence on design parameters is extracted.

II. Proposed Configuration

In energy-recovering systems, load capacitances (C_L) are typically driven by resonant sinusoidal waves which charge nodes and recover part of the charge in the falling half-period of the wave. It can be proven [6] that if a resistive load R is present in the current flow path, the energy dissipated on that load during a full charge/discharge cycle ($\frac{1}{f}$) would be:

$$E_{DISS} = \frac{\pi^2}{2}(RC_L f)C_L V_{DD}^2 \quad (1)$$

If an equivalent capacitive load was driven by conventional CMOS logic while switching at the same frequency f, the energy dissipation per cycle would be:

$$E_{CONV} = \frac{1}{2}C_L V_{DD}^2 \quad (2)$$

Therefore, as long as the switching frequency is $f < \frac{1}{\pi^2 RC_L}$, energy-recovering designs can save energy when compared to conventional CMOS logic.

In a 3D IC, TSVs will provide an interconnection path for signals crossing adjacent tiers. Since TSVs can have an appreciable parasitic capacitance [7], which will increase as additional TSVs are connected in series, ratioed buffer stages will be required so as to ensure a sharp-rising signal at the output of the TSVs. To reduce energy dissipation, an energy-recovering configuration could replace the required buffering stages allowing only sinusoidal signals crossing TSVs and thus saving energy according to (1).

In the proposed 3D interconnecting configuration (Figure 1), each tier is clocked with the assistance of conventional buffer stages whereas data signals, prior to crossing a TSV, are converted to sinusoidal waves with the use of adiabatic drivers (Figure 2).

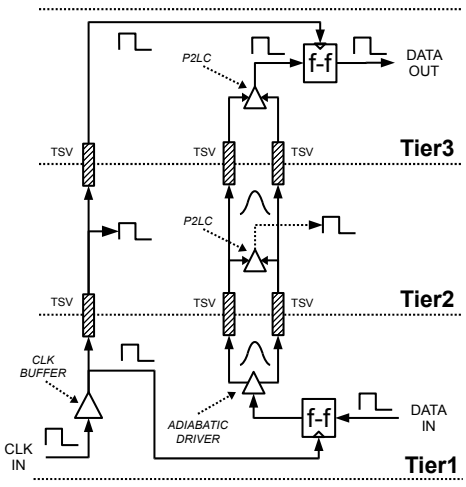

Figure 1. Proposed configuration.

The excellent energy efficiency of sinusoidal charging and energy recovery can considerably reduce energy dissipation for interconnecting signals. At the same time, compatibility with digital logic is retained by converting locally in each tier,

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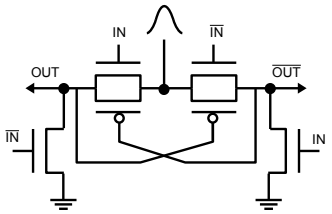

Figure 2. Adiabatic driver.

the resulting sinusoidal dual-rail pulses back to level signals through Pulse-to-Level converters (P2LC) (Figure 3).

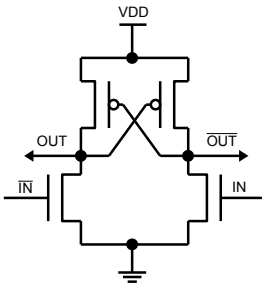

Figure 3. A Pulse-to-Level Converter implementation.

III. Analysis

Sinusoidal waveforms can be efficiently generated with the use of a single resonant-tank inductor [8], which when combined with the adiabatic driver's resistance (R_{TG}) and the TSV capacitance (C_{TSV}), forms an RLC oscillator (Figure 4) resonating at:

$$f = \frac{1}{2\pi\sqrt{L_{ind}C_{TSV}}} \tag{3}$$

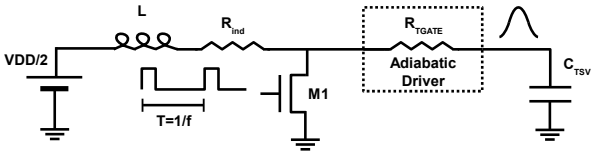

Figure 4. Resonant pulse generator.

The bulk of the energy dissipation in the proposed configuration will occur on the adiabatic driver, the inductor's parasitic resistance (R_{ind}) and transistor M1. Since the sinusoidal pulses will have to be converted back to level-signals after crossing a TSV, the P2L converters will contribute to the total energy dissipation as well.

A. Adiabatic driver

The adiabatic driver used in this configuration (Figure 2) is based on adiabatic circuits presented in [9], [10], with the load capacitance replaced by the parasitic capacitance of TSVs (C_{TSV}).

Energy in the adiabatic driver is dissipated both on the transmission-gate resistance (R_{TG}) and for driving its input capacitance. Assuming that both nFET and pFET transistors are equally sized (W_n), the cross-coupled pFETs reduce the conventionally-driven input capacitance by ½, however their gate capacitance (C_n) will appear as an additional capacitive load to the driver. Furthermore, drain/source diffusion capacitance (C_D) can be an important portion of the load since in each cycle $6C_D$ will be present in the current flow path (4 contributed by the ON T-gate and 2 by the OFF T-gate).

Therefore the combined load capacitance will be:

$$C_L = C_{TSV} + C_n + 6C_D \tag{4}$$

The resistance of the T-gate (R_{TG}) can be related to the gate capacitance by a "Device technology factor" (κ_{TG}) [11], which we can define for our convenience:

$$\kappa_{TG} = R_{TG}C_n \rightarrow R_{TG} = \frac{\kappa_{TG}}{C_n} \tag{5}$$

Combining (1), (4) and (5) gives the total dissipated energy per cycle in the adiabatic driver:

$$E_{AD} = C_n V_{DD}^2 + \frac{\pi^2}{2}\frac{\kappa_{TG}}{C_n} f \left[C_{TSV} + C_n + 6C_D\right]^2 V_{DD}^2 \tag{6}$$

The second term of (6) has a consistent contribution to the energy dissipation on every cycle, while the first term is dependent on the data switching activity (D).

We can also further simplify this equation by defining the diffusion capacitance as a fraction of the input capacitance,

$$C_D = bC_n \tag{7}$$

and equating term $\frac{\pi^2}{2}\kappa_{TG}f$ to a variable,

$$y = \frac{\pi^2}{2}\kappa_{TG}f \tag{8}$$

Equation (6) then becomes:

$$\begin{aligned} E_{AD} &= D \cdot C_n V_{DD}^2 + \frac{y}{C_n}\left[C_{TSV} + (6b+1)C_n\right]^2 V_{DD}^2 \\ &= \left[C_n\left(\frac{D}{y} + (6b+1)^2\right) + \frac{1}{C_n}C_{TSV}^2\right] \cdot yV_{DD}^2 \\ &\quad + (12b+2)C_{TSV} \cdot yV_{DD}^2 \end{aligned} \tag{9}$$

Since in (9) C_n is the free parameter, the first two terms of (9) are inversely proportional and E_{AD} is minimized when they become equal. The value of the gate capacitance at that point is calculated as:

$$C_{n(opt)} = \sqrt{[\frac{D}{y} + (6b+1)^2]^{-1}}C_{TSV} \tag{10}$$

Combining (9) and (10) results in minimum energy dissipation for the adiabatic driver, which is:

$$E_{AD(min)} = \left[\sqrt{\frac{D}{y} + (6b+1)^2} + (6b+1)\right] \cdot 2yC_{TSV}V_{DD}^2 \tag{11}$$

Replacing variable y in (11), we can observe the dependence of the energy dissipation on parameters f and κ_{TG}:

$$\begin{aligned} E_{AD} &= \left[\sqrt{\frac{2D}{\pi^2\kappa_{TG}f} + (6b+1)^2} + (6b+1)\right] \\ &\quad \cdot \pi^2\kappa_{TG}fC_{TSV}V_{DD}^2 \end{aligned} \tag{12}$$

B. Switch M1

Respectively, the energy dissipation on M1 which is switched-on briefly to recover the energy dissipated each cycle on the $R_{total} = R_{TG} + R_{ind}$, is a trade-off between dissipation on its on-resistance R_{M1} and input capacitance C_{M1}. Since M1 is a fairly large transistor, previous ratioed stages will have a significant energy consumption. For that reason a m factor is used to compensate for the additional losses. $I_{M1(rms)}$ is the rms current passing through the transistor while turned-on and V_{GM1} is the peak gate voltage. A methodology for deriving optimum values for both these parameters is proposed in [8].

The total dissipated energy on M1 can be calculated as:

$$E_{M1} = mC_{M1}V_{GM1}^2 + \frac{I_{M1(rms)}^2 R_{M1}}{f} \tag{13}$$

For transistor M1 we can also define a "Device technology factor":

$$\kappa_{M1} = R_{M1}C_{M1} \Rightarrow R_{M1} = \frac{\kappa_{M1}}{C_{M1}} \tag{14}$$

Substituting R_{M1} into (13):

$$E_{M1} = mC_{M1}V_{GM1}^2 + \frac{1}{C_{M1}}\frac{I_{M1(rms)}^2 \kappa_{M1}}{f} \tag{15}$$

Minimum energy consumption will occur when the two terms of (15) are equal:

$$C_{M1(opt)} = \sqrt{\frac{\kappa_{M1}}{mf}}\frac{I_{M1(rms)}}{V_{GM1}} \tag{16}$$

$$E_{M1(min)} = 2I_{M1(rms)}V_{GM1}\sqrt{\frac{m\kappa_{M1}}{f}} \tag{17}$$

C. Inductor's parasitic resistance

The inductor's (L_{ind}) parasitic resistance R_{ind} is proportional to the Q_{ind} factor, which is typically implementation technology dependent. For the purposes of this analysis it can be estimated as:

$$\begin{aligned} Q_{ind} &= \frac{1}{R_{ind}}\sqrt{\frac{L_{ind}}{C_L}} \\ \Rightarrow R_{ind} &= \frac{1}{Q_{ind}}\sqrt{\frac{L_{ind}}{C_L}} \\ \Rightarrow R_{ind} &= \frac{1}{Q_{ind}C_L 2\pi f} \end{aligned} \tag{18}$$

Energy dissipation on R_{ind} can be estimated using (1) as:

$$E_{ind} = \frac{\pi^2}{2}\left(R_{ind}C_L f\right)C_L V_{DD}^2 \tag{19}$$

Combining (18) and (19) we calculate the inductor's energy dependence on the Q_{ind} factor:

$$E_{ind} = \frac{\pi}{4}\frac{C_L}{Q_{ind}}V_{DD}^2 \tag{20}$$

D. Total energy dissipation

The total dissipated energy for the adiabatic driver, switch M1 and inductor's resistance can be calculated by combining (12), (17) and (20):

$$E_{total} = E_{AD} + E_{M1} + E_{ind} \tag{21}$$

Nevertheless, for (21) to be complete the energy contribution of the P2L converters has to be included as well, which cannot be theoretically derived and is addressed in the following sections.

IV. Evaluation

For the evaluation of the proposed method, the κ_{TG}, κ_{M1} and C_D parameters were extracted using simulation models for a 130nm process. The TSV capacitance was assumed to be 160fF, a value which can be either derived from a single TSV or a series combination of TSVs distributed among subsequent tiers in a 3D IC. The supply voltage was at 1.2V and data switching activity was assumed to be equal to 1.

All parameters were inserted into (21) and the energy dissipation per bit per cycle was calculated, with the operating frequency and Q factor as free variables. An identical circuit configuration was simulated as well in a commercial SPICE program and the simulation data showed good correlation with the theoretical estimations.

The inductor's quality factor can have a considerable effect on the energy dissipation and this can be observed in Figure 5, where the estimated energy dissipation is plotted for various operating frequencies.

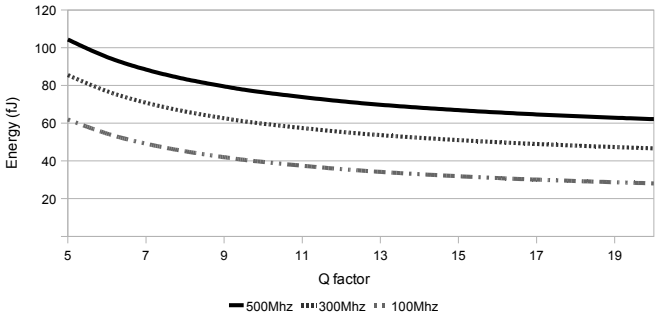

Figure 5. Estimated energy dissipation at 500, 200, 100 MHz. TSV=160fF.

V. Comparison

The proposed configuration was compared to a conventional CMOS buffer with ratioed stages driving an equivalent TSV load capacitance. Since the conventional buffer when transmitting data will produce just one charging event per 2 cycles of the operating frequency, its energy dissipation per cycle is calculated as in (2). If we also include the data switching activity, then:

$$E_{CONV} = D \cdot \frac{1}{2}C_L V_{DD}^2 \tag{22}$$

The estimated energy performance improvement of the proposed configuration over the conventional buffer for $D = 1$, can be seen in Figure 6.

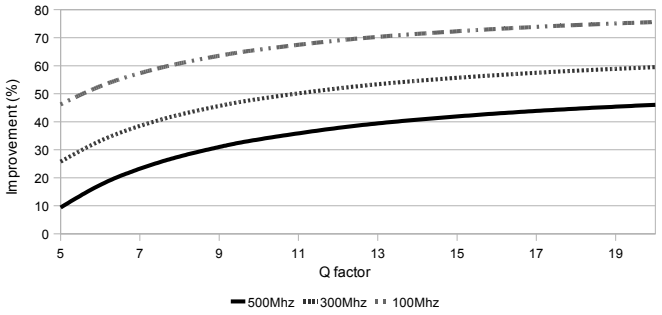

Figure 6. Energy performance improvement of the proposed energy-recovering configuration over a conventional buffer driving an equivalent TSV load capacitance.

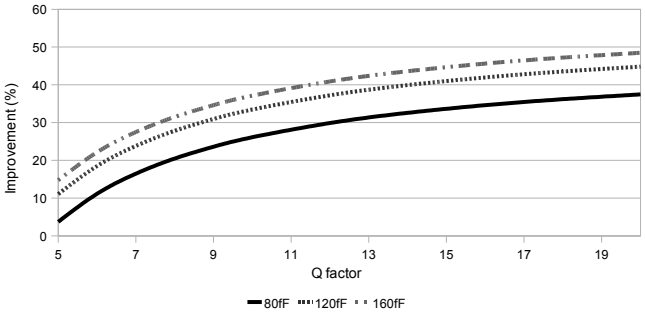

Figure 7. Energy dissipation reduction at 300MHz when P2LC is included and the TSV load is variable.

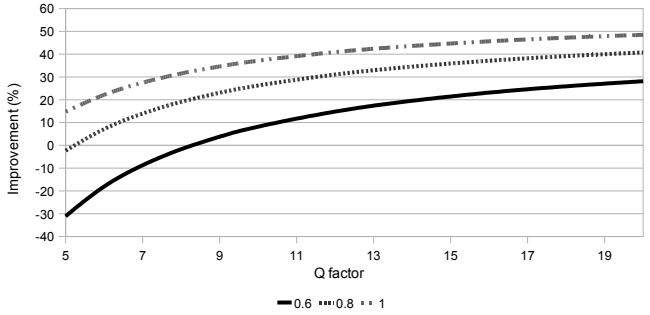

Figure 8. Improvement in energy dissipation when P2LC is included and switching activity is variable. f=300MHz, TSV=160fF.

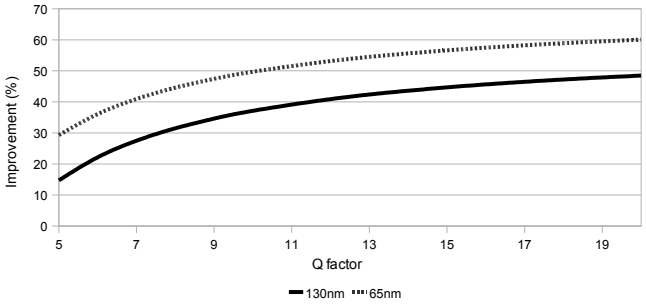

Figure 9. Improvement in energy dissipation when P2LC is included and process technology is variable. f=300MHz, TSV=160fF.

Varying the value of the TSV load capacitance has no effect on the estimated energy improvement percentage, as the energy dissipation for both the proposed method and the conventional buffer is linearly related to the load capacitance. However, the data plotted in Figures 5, 6 can be considered as the theoretical maximum performance attainable by the energy-recovering method, since the energy dissipation of the P2L converters is not included in these estimations.

To include the effect of the P2L converters in the energy calculations, a simple circuit topology is chosen (Figure 3) and its energy dissipation is extracted from simulation data. Since the P2L converter has constant energy dissipation regardless of the value of the TSV capacitance, the linear relation of the total dissipated energy to the load capacitance value is no longer valid for the energy-recovering circuit. This can be observed in Figure 7, where the estimated energy improvement is plotted at 300MHz operating frequency and the TSV load capacitance is variable. It can be expected that as the load capacitance increases, energy performance would approach the estimations in Figure 6.

Switching activity can also be a significant factor affecting energy performance. Since in the energy-recovering circuit the sinewave oscillation cannot be halted, all capacitances in the current flow path will charge and discharge on each cycle regardless of data activity. In contrast, static CMOS ideally dissipates energy only when switching and thus the energy-recovering circuit can compare favorably only at high switching rates. In Figure 8, the estimated effect of the switching activity on energy performance is plotted for an operating frequency of 300Mhz.

Since the technology factors κ_{TG} and κ_{M1} were extracted for the 130nm process, reducing their value by ½ could also provide us with an estimation of the circuit's energy performance for the 65nm node. The result in plotted in Figure 9 and as can be observed, technology scaling has a positive effect on energy dissipation when compared to the conventional buffer.

VI. Conclusions

In this work, a theoretical analysis was developed to investigate the potential of the energy-recovering methodology, as used in adiabatic logic and resonant clock distribution networks, for reducing the energy dissipation of 3D IC interconnects. The total energy dissipation per cycle and optimum device sizing were extracted for the proposed method using the theoretical models. Simulation data showed good correlation with the theoretical estimations on a 130nm process.

The proposed configuration was compared against a conventional CMOS buffer, driving an equivalent TSV load capacitance and its energy performance was evaluated. Analysis revealed energy dependence on Q, f, D and TSV capacitance parameters and the results demonstrated favorable energy performance for high Q factors/switching activities/TSV capacitances and low operating frequencies. Furthermore, an estimation was provided on the energy performance behavior of the energy-recovering design in an advanced technology node, where improved efficiency was demonstrated.

REFERENCES

[1] H. Mahmoodi, V. Tirumalashetty, M. Cooke and K. Roy, "Ultra Low-Power Clocking Scheme Using Energy Recovery and Clock Gating", IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Jan. 2009, Volume: 17, Issue 1, pp. 33-44.

[2] M. Facchini et al., "System-level Power/performance Evaluation of 3D stacked DRAMs for Mobile Applications", 2009, Design, Automation, and Test in Europe (DATE) conference 2009.

[3] C. L. Seitz et al., "Hot Clock nMOS", Technical Report, California Institute of Technology, 1985, [CaltechCSTR:1985.5177-tr-85].

[4] S. Kim, C. H. Ziesler, M. C. Papaefthymiou, "Charge-Recovery Computing on Silicon", IEEE Trans. Computers 54(6): 651-659 (2005).

[5] V. S. Sathe, J. C. Kao and M. C. Papaefthymiou, "Resonant-Clock Latch-Based Design", IEEE Journal of Solid-State Circuits, Volume 43, Issue 4, April 2008, pp. 864 - 873.

[6] B. Voss and M. Glesner, "A low power sinusoidal clock", The 2001 IEEE International Symposium on Circuits and Systems, Volume 4, 6-9 May 2001, pp. 108 - 111, vol. 4.

[7] P. Marchal et al., "3D Technology Assessment: Path-finding the technology/Design Sweet-spot", Proceedings of the IEEE, January 2009, vol 97, pp. 96-107.

[8] D. Maksimovic, V. G. Oklobdzija, "Integrated power clock generators for low energy logic", 26th Annual IEEE Power Electronics Specialists Conference, 18-22 Jun 1995, pp. 61-67, vol.1.

[9] W. C. Athas, L. J. Svensson, J. G. Koller, N. Tzartzanis, and E. YC. Chou, "Low-power digital systems based on adiabatic-switching principles", IEEE Trans. Very Large Scale Intgr. (VLSI) Syst., vol. 2, no. 4, pp. 398407, April 1994.

[10] C. C. Yeh, J. H. Lou, and J. B. Kuo, "1.5V CMOS Full-Swing Energy Efficient Logic (EEL) Circuit Suitable for Low-Voltage and Low-Power VLSI Application," Elec. Lett., Vol. 33, No. 16, pp. 1375-1376, 1997.

[11] D. Maksimovic, "A MOS gate drive with resonant transitions", 22nd Annual IEEE Power Electronics Specialists Conference, 24-27 Jun 1991, pp.527-532.