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Experimental Observation of Negative Capacitance in Ferroelectrics at Room Temperature

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ABSTRACT: Effective negative capacitance has been postulated in ferroelectrics because there is a hysteresis in plots of polarization-electric field. Compelling experimental evidence of effective negative capacitance is presented here at room temperature in engineered devices, where it is stabilized by the presence of a paraelectric material. In future integrated circuits, the incorporation of such negative capacitance into MOSFET gate stacks would reduce the subthreshold slope, enabling low power operation and reduced self-heating.

The concept of ferroelectrics displaying effective negative permittivity has led to the speculation that its inclusion in the gate stack of a metal oxide semiconductor field effect transistor (MOSFET) will reduce the subthreshold swing of complementary metal oxide semiconductor (CMOS) devices below 60 mV/dec. For a gate stack comprising a thin ferroelectric layer on top of a thin insulator layer, the channel potential ($\Psi$) can change more than the gate voltage ($V_g$) thus providing a step-up voltage transformer and $S < 60$ mV/dec. If this can be engineered, it heralds a transformation of future integrated circuits (ICs), reducing the overall power operation and reduced self-heating.

Attempts have been made to observe experimentally the characteristics of negative capacitance in ferroelectrics. However, this has proven elusive for ferroelectrics in isolation, because it corresponds with a negative energy density and so is unstable. In order to observe negative capacitance, it must be incorporated into a device with overall positive capacitance (and therefore positive energy density). Specifically, negative capacitance can be stabilized by using a bilayer metal–insulator–metal (MIM) parallel plate capacitor, as shown in Figure 1a.

The total capacitance $C_T$ is the sum of the inverse capacitances of each layer

$$\frac{1}{C_T} = \frac{1}{C_1} + \frac{1}{C_2}$$

where $C_1$ is the capacitance of a paraelectric material and $C_3$ is the capacitance of a ferroelectric material. Figure 1b shows the theoretical relationship between $C_T$, $C_1$ and $C_2$ based on eq 1. It is observed that as $C_T$ varies from positive to negative, $C_T$ undergoes different changes to its overall stability. Region b is...
identified as the design window where effective negative capacitance is stabilized, corresponding with a positive total energy density. Moreover, the total capacitance $C_T$ is larger than the constituent positive capacitance $C_1$ due to the negative capacitance $C_2$. Region a is unstable, as it has a total energy density that is negative, while region c comprises two positive capacitances in series that combine to have a reduced total capacitance.

In order to provide a better understanding of this phenomenon, the relationship between the total energy density and negative capacitance is described. The ability of a body to store electrical charge, $Q$, is defined by its capacitance, $C$. It can be described in terms of a change in energy density, $U$, as a function of changes in stored charge, $Q$

$$C = \left[ \frac{d^2U}{dQ^2} \right]^{-1} \tag{2}$$

Thus, for a conventional dielectric there is a quadratic relation between energy density and charge, or polarization. For paraelectric material, where the relation between polarization and applied electric field is nonlinear, the relation between energy density and polarization still has a single turning point when $P = 0$. Ferroelectric materials exhibit a spontaneous electric polarization below a critical temperature, $T_c$. Hysteresis is seen in plots of polarization versus applied electric field. It arises from an increasing alignment of electric dipoles as the applied electric field increases, which increases the polarization; when the field is removed there is a nonzero remnant polarization. This is manifested in plots of energy density versus polarization by two minima, as shown in Figure 2a for $C_2$. The stabilized minima ensure capacitance is always positive for a ferroelectric under the critical temperature, and polarization switching occurs when the field is reversed (Supporting Information, Figure S1a,b). The negative capacitance region (dashed box in Figure 2a) described by eq 2 due to the negative energy curvature is unstable in isolation. Hence, negative capacitance is never measured for single layer ferroelectrics and should be stabilized in a series capacitance system. 4

Effective negative capacitance may only be inferred from experiment using specific bilayer MIM device designs and conditions, as described above. Figure 2 shows energy density as a function of polarization for a bilayer $C_T$ of SrTiO$_3$, which is paraelectric and has a capacitance $C_1$, and BaTiO$_3$, which is ferroelectric below the Curie temperature, $T_c$, and has a capacitance $C_2$. The relationship between $C_T$, $C_1$, and $C_2$ has been shown previously in eq 1. The series configuration of capacitances allows the summation of the constituent energy
functions to create an overall energy density for \( C_T \) (details in Supporting Information, Figure S1).

At a low temperature of 100 K (Figure 2a), the total capacitance displays ferroelectric properties as seen by the double minima for the total capacitance \( C_T \). As a result, the negative capacitance will be energetically unstable and not observable. This corresponds to operations in region a, as shown in Figure 1b. At room temperature (Figure 2b), this bilayer design shows an overall positive capacitance as seen by the single minimum in \( C_T \) at \( P = 0 \) and so negative capacitance could be observed. This is the ideal stable operation window, as described in region b in Figure 1b. At a temperature of 500 K (Figure 2c), above \( T_c \) the BaTiO3 layer has become paraelectric and so the overall capacitance comes from two paraelectric contributions. In this case, it follows that the total capacitance \( C_T \) is less than \( C_1 \) or \( C_2 \), corresponding to region c in Figure 1b.

For the capacitor shown in Figure 2b where \( C_T \) is negative, then \( C_T \) can become larger than \( C_1 \). In this study, experimental evidence is presented to demonstrate effective negative capacitance at room temperature in a thin film of the ferroelectric BaTiO3. The BaTiO3 is fabricated in a bilayer stack in series with SrTiO3, which is paraelectric at room temperature. The MIM stack is formed on a SrTiO3 substrate and using SrRuO3 as the bottom conducting electrode, which is lattice matched to the substrate.

SrTiO3, BaTiO3, and SrRuO3 layers used for this study were all deposited by pulsed laser deposition (PLD) technique with a KrF excimer laser from Lambda Physik. Prior to PLD, commercially available, one side polished, single crystal [100] oriented SrTiO3 substrates of 1 cm x 1 cm were cleaned. The cleaning procedure involved an ultrasonic bath in acetone, isopropanol, and deionized water for 3 min each. The bottom electrodes (SrRuO3) were deposited at 700 °C at an oxygen pressure of 75 mTorr. A corner of the sample was covered with a small drop of TiO2 solution in acetone and was allowed to dry at room temperature. The purpose of this was to give access to the bottom electrode for electrical measurements. SrTiO3 and BaTiO3 layers were deposited at a substrate temperature of 850 °C and 75 mTorr oxygen pressure without breaking the vacuum of the PLD chamber. TiO2 was then gently scratched away and the sample was again rinsed in acetone, isopropanol, and deionized water. Circular patterns for top electrodes were created by spinning photoresist AZ-5214E, exposing using Karl-Suss MJ83 aligner and developing in AZ-326 MIF. A 60 nm thick Pt was deposited using a BOC-Edwards electron-beam evaporator and lifted-off in N-methylpyrrolidone. Electrodes of sizes ranging from 50 to 300 μm were thus fabricated to complete the MIM capacitor structure. The SrTiO3 thickness is 25 nm and capacitors having BaTiO3 thicknesses of 0, 20, 30, and 50 nm were investigated. An additional BaTiO3 capacitor of thickness 30 nm was deposited without a 25 nm SrTiO3 layer.

Capacitance–voltage (CV) measurements on an Agilent 4294A system were taken at room temperature at a frequency of 10 kHz. Frequency was also varied between 1 kHz and 1 MHz to measure capacitance across a wide frequency range. XRD spectra were acquired using Panalytical x’pert Pro with Cu Kα X-ray radiation having a characteristic wavelength of 1.5418 Å. Transmission electron microscopy was conducted on a JEOL-2100F microscope operating a 200 kV Schottky field emitter. Electron diffractions were processed using Fourier transforms in the Gatan DigitalMicrograph software.

Cross sections of each interface of the capacitor having a BaTiO3 thickness of 20 nm are shown in Figure 3. Each layer is perovskite and grown epitaxially, lattice matched to the SrTiO3 (100) substrate. Electron diffraction (EDX), and X-ray diffraction (Supporting Information, Figures S2, S3) confirm a single crystal orientation throughout the MIM stack. Atomic force microscopy confirms the smooth interface due to the lattice-matched materials (Supporting Information, Figure S4). Reciprocal space mapping of the EDX pattern in Figure 3a indicates a lattice constant ratio of the perpendicular and in-plane parameters, \( c/a = 1.07 \). An elongation of the \( c \) lattice parameter favors the ferroelectric phase in the BaTiO3 film and is necessary for the negative capacitance observed in each structure. The remaining SrTiO3 and SrRuO3 films were cubic, \( c/a = 1 \).

In Figure 4a, the total capacitance for each capacitor is plotted as a function of their BaTiO3 layer thickness. A data point representing the single BaTiO3 capacitor \( C_2 \) of thickness 30 nm without the 25 nm SrTiO3 layer is also shown for comparison. As the BaTiO3 layer thickness increases then the
total capacitance is seen to increase, which is consistent with the ferroelectric capacitance being negative ($C_f$ being negative in eq 1 and so $C_t$ increases). The increase in ferroelectric layer thickness corresponds with $C_f$ decreasing in magnitude, so the trend in experiment is consistent with Figure 1b. In each case, the bilayer capacitance exceeds the SrTiO$_3$ capacitance alone. Any hysteresis behavior is absent from the capacitance measurements in these bilayer devices, which show tunable paraelectric capacitance properties (Figure 4b), consistent with the single minimum energy function in Figure 1b. At 30 nm thickness, in Figure 4a the BaTiO$_3$ capacitance $C_f$ displays lower capacitance than in the bilayer. Incorporation of the 25 nm SrTiO$_3$ thickness has led to an increase in total capacitance due to the stabilized negative capacitance layer in the bilayer (further detail in Supporting Information, Figure S1a,b). The tunable capacitance trends are also shown to increase in Figure 4b as the thickness of BaTiO$_3$ increases. This is consistent with the insulator becoming dominated with BaTiO$_3$ due to its higher Curie temperature $T_c$. The quality of BaTiO$_3$ was verified using the single 30 nm layer deposited on SrRuO$_3$ and investigated using piezoforce microscopy (Supporting Information, Figure S6).

The relative permittivity for bulk SrTiO$_3$ is widely reported$^7$ to be around 300, while it is lower for nanometer scale thin films of SrTiO$_3$ $^8$ (relative permittivity for 25 nm SrTiO$_3$ capacitor $C_f$ is 200). Using this bulk value for SrTiO$_3$ permittivity, the capacitance of the 25 nm SrTiO$_3$ layer is included as a dashed line in Figure 4a. Even for this most conservative estimate of SrTiO$_3$ permittivity, the total capacitance for the bilayer stack having a BaTiO$_3$ layer 50 nm thick is larger than with SrTiO$_3$ alone, which indicates an effective negative capacitance for the BaTiO$_3$ layer. This comparison rules out the possibility of the capacitance enhancement resulting from a dead layer effect in the 25 nm SrTiO$_3$ capacitor, which may otherwise lead to incorrect assumptions about the capacitance enhancement.$^9$ It also discounts any leakage-mediated reductions in capacitance measured on the single layer SrTiO$_3$ capacitor and points to the increased total capacitance arising from the stabilization of BaTiO$_3$ negative capacitance.

The Maxwell–Wagner effect is known to cause dielectric permittivity enhancement in superlattices,$^{10}$ and evidence of this in BaTiO$_3$/SrTiO$_3$ heterostructures has been reported previously.$^{11}$ But the Maxwell–Wagner effect is known to correlate with the number of heterojunction interfaces and reduces at low frequency. This explanation is therefore not relevant for the capacitance enhancement reported here, which only has a single interface. Moreover, electrical measurements carried out up to 1 MHz also showed capacitance enhancement in these bilayers (Supporting Information, Figure S5). This further rules out Maxwell–Wagner effects as well as defect mediated influences.

The greatest challenge facing nanoelectronics scaling is power dissipation in MOSFETs. Using existing CMOS technology, the subthreshold slope in the transfer characteristic is 60 mV/decade of current (or larger). Thus, for a given on-state current requirement this imposes a limit on either the on-state voltage or the off-state current. The incorporation of effective negative capacitance in the gate stack has been proposed$^{1,6}$ to overcome this barrier and experimental investigations have been reported. For example, MOSFET's incorporating polymer ferroelectrics in the gate stack demonstrate a subthreshold swing less than 60 mV/decade over limited current ranges below $10^{-10}$ A/um, compared with a typical MOSFET threshold current of $10^{-7}$ A/um.$^{7,12,13}$ These studies showed hysteretic electrical characteristics, which does not correspond to fully stabilized ferroelectric layers as shown in the present work. However, the results indicate the likelihood of negative capacitance as a technology for reducing the subthreshold swing. Similarly, a 2.5 nm layer of AlInN in the gate stack of a metal oxide semiconductor high electron mobility transistor (MOS-HEMT) shows a reduced subthreshold slope, but again only over a restricted current range below $10^{-11}$ A and believed to be due to polarization effects.$^{14}$ The structure also required an ultrathin 2.5 nm layer of AlInN with lateral compositional gradients, and the reduced subthreshold slope was lost at a thickness of 7 nm.

A study using the perovskite ferroelectric Pb(Zr$_{0.2}$Ti$_{0.8}$)O$_3$ in a previous bilayer capacitors has been shown.$^{15}$ Negative capacitance was stabilized across a temperature range exceeding 573 K, and therefore is unsuitable for integration into modern integrated circuits. Furthermore, stabilization was shown at temperatures up to 773 K and beyond the Curie temperature of the ferroelectric.$^{16}$ Explanations for this may be due to straining as the latticed matched structures impose strains that lead to increases in the Curie temperature; however, this was not discussed in the study. The study highlighted that using low Curie temperature materials will enable negative capacitance stabilization at room temperature, such as BaTiO$_3$ used here.

The present work demonstrates the feasibility of negative capacitance at room temperature using a lead-free perovskite ferroelectric of varying thickness. The robust material can be integrated into CMOS or included as a performance booster within innovative devices such as tunnel field effect transistors$^3$ in order to realize a future low power technology.

### ASSOCIATED CONTENT

#### Supporting Information

Details on bilayer design and additional simulations. Further experimental evidence of negative capacitance and bilayer material quality. This material is available free of charge via the Internet at http://pubs.acs.org.
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The manuscript was written through contributions of all authors. All authors have given approval to the final version of the manuscript.

**Notes**
The authors declare no competing financial interest.

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