Al-Daloo M, Yakovlev A, Halak B.

Energy Efficient Bootstrapped CMOS Inverter for Ultra-Low Power Applications.

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Energy Efficient Bootstrapped CMOS Inverter for Ultra-Low Power Applications

Mohammed Al-daloo and Alex Yakovlev
School of Electrical and Electronic Engineering
Newcastle University
Newcastle upon Tyne, UK
Email: m.i.t.tawfeeq, Alex.Yakovlev@ncl.ac.uk

Basel Halak
School of Electronics and Computer Science
University of Southampton
Southampton, UK
Email: bh9@ecs.soton.ac.uk

***Abstract*—This paper describes an energy efficient bootstrapped CMOS inverter for ultra-low power applications. The proposed design is achieved by internally boosting the gate voltage of the transistors (via the charge pumping technique), and the operating region is shifted from the sub-threshold to a higher region, enhancing performance and improving tolerance to PVT variations. The proposed bootstrapped driver uses fewer transistors operating in the sub-threshold region, and consists of two stages. The first stage is a normal driver with PMOS and NMOS transistors that are driven by the enhancing voltage circuit (stage 2) which generates voltage levels theoretically between -V_{DD} for pulling up to 2V_{DD} for pulling down. Our analysis shows that the proposed implementation achieves around 20% reduction in energy consumption compared to conventional designs under a supply voltage of 0.15V V_{DD}.**

***Index Terms*—ultra-low power (ULP); interconnect; charge pump; driver; boosting.**

I. Introduction

The rapid development of energy-constrained applications has made low power design, a primary concern. This is a paradigm shift from traditional performance-led design to emerging energy-constrained system development. Novel applications such as IoT devices, wearable computing and smart grids mainly require longer energy source life and small silicon costs; on the other hand, their performance is typically considered a secondary concern.

Recently, scaling the power supply has become an effective way to reduce energy consumption in digital systems. Supply voltages less than the threshold voltage of the CMOS (complementary metal-oxide semiconductor) circuits have emerged showing the ability to meet the requirements of ultra-low power regime (ULP). This approach is called the sub-threshold logic circuit. However, since CMOS scaling reaching its limits, the issue of global and long interconnects has become an important consideration for circuits in high speed systems due to the problem of capacitance [1].

At sub-threshold this effect is even worse, for instance, when the conventional CMOS driver needs to be as large as possible to deal with the leak of driving efficiency associated with a scaled power supply [2]; in addition, it requires to bear with a static current I_{off} issue which is increasing at this region, particularly, in the nanometre regime [3].

In this paper, the bootstrap method is proposed because of its capability to improve the driving ability without increasing the circuit power consumed, as shown below in the results section. The bootstrapped CMOS inverter provides better performance and reduces leakage current by producing a voltage swing nearly of $2V_{DD}$ to -V_{DD} and driving the V_{gs} (gate to source transistor voltage) of the NMOS and PMOS respectively. Hence, according to the formula for I-V in a sub-threshold regoin [4], [5], I_{off} will be reduced exponentially.

The rest of the paper is organized as follows. Section II introduces the operation of the circuit and its structure. Section III describes implementation considerations and presents the circuit design and initial simulation results for this circuit and compares it with previous designs [2] and [6], as well as with a conventional driver from the point of view of energy consumption and delay. In addition, the conclusions are presented in section IV.

II. Proposed CMOS Inverter

A. Charge pump technique

In our approach, the bootstrap has been used based on a charge pump that is a type of DC-to-DC converter, which utilities a capacitor as charge holder to generate a voltage higher than the power source voltage [7]. Although the design of this technique is electrically a simple circuit, it is able to achieve a level of efficiency reaching 90-95% [8]. To see how this is possible, consider a simple 4-stages Dickson charge pump as shown in figure 1. When the signal $\phi1$ is low, D1 will charge C1 to V_{in}. When $\phi1$ goes high, the top plate of C1 is pushed up to $2V_{in}$. D1 is then turned off and D2 turned on and C2 begins to charge to $2V_{in}$. On the next clock cycle, $\phi1$ again goes low and now $\phi2$ goes high, the top plate of C2 is pushed to $3V_{in}$. D2 switches off and D3 switches on, charging C3 to $3V_{in}$ and so on with charge passing up the chain hence, the name 'charge pump'. The final diode-capacitor cell represents a peak detector and not a multiplier in the cascade [8].

However, this technique increases the supply voltage efficiently, and this only includes the positive part of the voltage; that is, Vo will swing just from 0 to 2 or 3 V_{in}. So we have modified the cross-coupled MOSFET voltage doubler to give a full swing from -V_{DD} to $2V_{DD}$. The schematic of our approach is highlighted in figure 2.

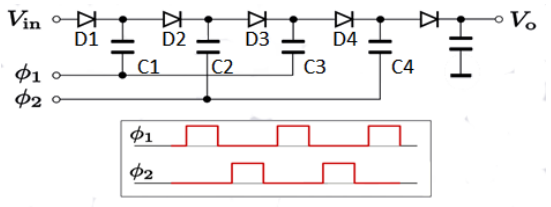

Fig. 1. Four-stages Dickson charge pump [8].

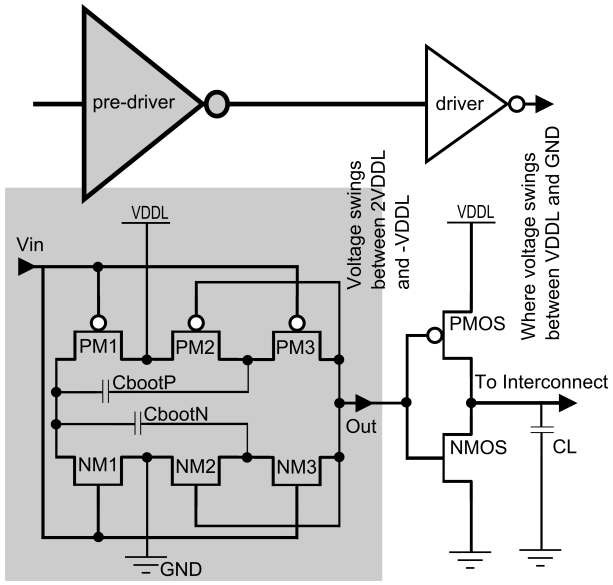

Fig. 2. Circuit of the proposed driver.

The ideal operation of the circuit is divided into two states. The first state is when V_{in} goes low, that pushes PM1, PM3 and NM2 on, and thus C_{bootN} is charged to -V_{DD}. At the same time, the supply voltage V_{DD} together with C_{bootP} voltage is pulling up to $2V_{DD}$ the voltage of the output, where strongly switch off the PM2 and any PMOS connected to this terminal (Out). A similar but opposite process takes place in the second state when V_{in} goes high; hence, NM1, NM3 and PM2 will be on, so C_{bootP} is charging to V_{DD} and inversely C_{bootN} charges to -V_{DD} which will appear on the output (Out) where yields PM2 switches on strongly and any PMOS connected to the circuit's output (Out). The size (W/L) of transistors (PM1, PM3, NM1 and NM3) is $200\,\mathrm{nm}/160\,\mathrm{nm}$ and (PM3 and NM3) is $120\,\mathrm{nm}/80\,\mathrm{nm}$.

We have used this approach to improve the driving capability of the CMOS circuits due to the increase in the sub-threshold swing which increases the driving current exponentially. In this report the charge pumper is used in the stage just before the interconnect driver, which means that its effect will be implicit; in other words, it will be used as a booster (bootstrap) for the final stage.

B. Circuit design

The bootstrap driver consists of two combinations. In general, the first one is a pre-driver that has the ability to theoretically provide a voltage swing between -V_{DD} and $2V_{DD}$ to enhance the driving capability of the next stage. The second stage is a normal buffer (inverter) with PMOS and NMOS transistors that are driven by the boosting voltage circuit. Figure 2 shows the circuit scheme of the proposed driver and its stages, where the pre-driver is the circuit in the middle which uses the capacitors to boost the voltage. Then the buffer, which is the circuit on the right, is used to drive the interconnect with a sub-threshold voltage swing from *GND* to V_{DD}.

C. Boosting efficiency

The capacity of the boost capacitance (C_{boost}) together with parasitic capacitance (C_{node}) of the transistors (PM2, PM3, NM2 and NM3) connected to the relevant node determines the efficiency of the boosting as in the following equations:

$$B = \frac{C_{boost}}{C_{boost} + C_{node}} \tag{1}$$

$$V_{gsn}(pulldown) = B \cdot 2V_{DD} \tag{2}$$

$$V_{gsp}(pullup) = B \cdot -V_{DD} \tag{3}$$

where the *B* is the booster efficiency factor, V_{gsn} is the gate-to-source of the N-type transistor, and V_{gsp} is the gate-to-source of the P-type transistor. Therefore, the efficiency of the boosting depends on the parasitic capacitance of the relevant transistors as well as the boosting capacitance which should be designed to be as large as possible to give better efficiency. Consequently, the ultimate stage of the driver circuit is pushed to a higher region owing to the boosted voltage, where the discharge current I_n in the components exposed to this voltage is:

$$I_n = \mu C_{dep} \frac{W}{L} \left((B \cdot 2V_{DD} - V_{th}) V_{DD} - 0.5V_{DD}^2 \right) \tag{4}$$

where μ denotes the effective mobility, C_{dep} is the depletion capacitance, *W* and *L* are the device width and length, and V_{th} is the threshold voltage. As a result, the boosted voltage increases the current driving capability. Moreover, not only is the discharge current affected but also the equivalent resistance (R_{eq}) of the MOS transistor will improve according to the following equation:

$$R_{eq} = \frac{V_{DS}}{I} = \frac{V_t}{\beta e^{\frac{-B \cdot V_{DD}}{V_t}}} \tag{5}$$

where β is the transistor strength, and *Vt* is the thermal voltage. So, depending on the above expression, the leakage current will decrease exponentially.

III. IMPLEMENTATION AND RESULTS

The driver circuit has been implemented using Cadence software in 90nm technology to measure the performance of the design. The circuit in figure 2 employs SPRVT transistor, 25 fF boost capacitors (C_{boost} and C_{node}), and 200 fF capacitance connected to the driver output (*CL*) to emulate the $10\,\mathrm{mm}$ interconnect. The simulation was executed under a $150\,\mathrm{mV}$

TABLE I
THE ACHIEVED VOLTAGE SWING AND BOOSTED COMPONENTS

Driver	Voltage swing	No. of boosted components
Conventional	normal (GND – V_{DD})	0
Proposed	full-swing (-V_{DD} – 2V_{DD})	4
[2]	full-swing (-V_{DD} – 2V_{DD})	2
[6]	half-swing (GND –2V_{DD})	2

supply voltage and 5 MHz frequency as the input frequency of the driver to imitate the worst case transition activity.

For ten clock cycles, the driver achieves average power and energy consumed of 24 nW and 47.9 fJ/10cycle respectively, with 85.5 pW leakage power and 10.5 ns/cycle input to output delay. In another study, the estimated results were 1 µW average power and 0.1 pJ/cycle with leakage power 107 nW and operating frequency reaching 10 MHz [2]. Furthermore, the results of [6] were 1.7 µW and 0.34 pJ for total average power and energy respectively, and 833 nW leakage power where, from the point of view of power leakage, this was the worst results so far among tested drivers. Even though the proposed driver achieves the best results for power saving and energy efficiency, it has not achieved the best recorded delay time which is normal as going deeper in sub-threshold voltage area. Owing to the number of components operating in the boosted voltage as shown in table I, the proposed design scheme performs better than other previous works.

Moreover, an investigation has been conducted to find the trade-off between the conventional buffer and the proposed design from the point of view of energy consumption and circuit delay. Thus, to run this comparison, we repeated the same experiments under the same circumstances except that the boosting technique was not used, in order to design the normal buffer in such a way as to be close to a bootstrap driver design. The results were as predicted, where the conventional buffer, with the same proposed circuit's transistors size where PMOS (NMOS) W/L is 800 nm/100 nm (650 nm/100 nm), does not have the capability to drive the same load (200 fF) with 150 mV as the supply voltage to obtain the same transient response as the design with boosting. The transient response results for the two drivers are demonstrated in figure 3.

So the solutions are either splitting the load into 8 parts and using repeaters for each part with 25 fF, or increasing the size of the normal buffer transistors so as to have the ability to drive this load. Regardless of which solution is chosen, the both situations lead to a power consumption increase. A large transistors buffer, which its transistors approximately 12 times larger than these in proposal design, where PMOS (NMOS) W/L is 12.5 µm/100 nm, has been implemented so as to give a fair comparison with the bootstrapped design, where the two drivers have been designed to have the same rise and fall output waveform response.

The results of the experiments have been obtained by implementing the UMC 90nm technology using the Cadence Spectre simulation toolkit.

The bootstrapped driver shows an improvement in energy

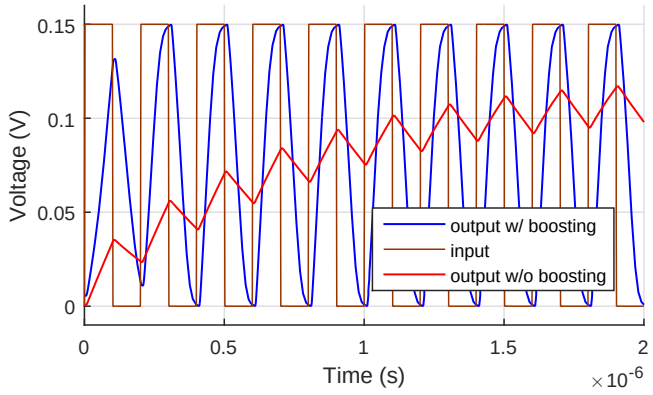

Fig. 3. Transient response waveform of drivers with same transistor size and circumstances.

TABLE II
SUMMARY OF COMPARISON RESULTS.

Item	Buffer without boosting	Buffer with boosting
Averge power (W)	31.45 n	25.37 n
Total energy (J/10cycle)	62.9 f	49.97 f
Chip area estimated (μm^2)	142.803	164.609
Load (CL) (F)	200 f	
Supply voltage V_{DD} (V)	150 m	

consumption which is 20% less than the conventional driver. Moreover, the driver without boosting consumes by 24% more power than the driver with boosting. This saving is due to the reduced leakage current which has a main role in the power dissipation of sub-threshold circuits. Table II lists the results of this comparison when the supply voltage is 150 mV, the load is 200 fF and the frequency is 5 MHz.

However, the improvements in power and energy consumption of the proposed driver are accompanied by greater chip area and circuit delay. Table II shows that the estimated chip area of the proposed driver is 164.609 µm^2 versus 142.803 µm^2 for the normal driver, which also gives lower input to output delay than the proposed design as shown in figure 4.

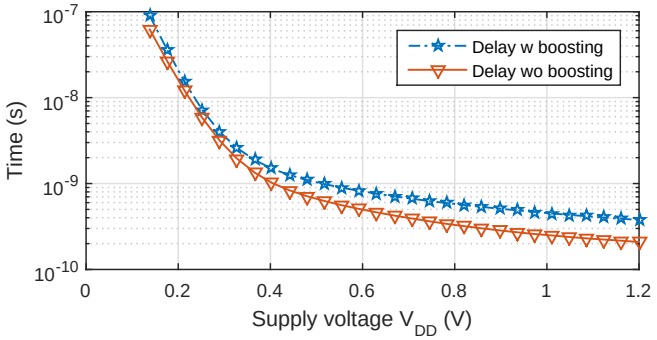

Fig. 4. Drivers with/without boosting delay with 200 fF load and 5 MHz frequency.

These results are normal from the area and delay point of view if it has realized that the bootstrapped driver has three stages practically, which are an embedded inverter in the booster stage, the pre-driver (booster) and the driver, in addition to the use of capacitors as shown in figure 2. Meanwhile the conventional driver is designed to have two stages, which are an inverter and a driver which require fewer but larger transistors. Despite that, the main consideration in this report is not the delay but the energy savings which have been achieved by using a boosting technique.

Another perspective is that of the buffer's consumption of energy, which is shown in figure 5. Generally, the figure provides the outcome of these experiments where the supply voltage has been changed from deep sub-threshold to near super-threshold voltage, which obviously shows the advantage of the buffer with boosting compared to the one without boosting.

Furthermore, figures 6 and 7 show the improvements of the bootstrapped driver compared to the normal driver from the points of view of leakage power and energy efficiency which is, in this paper, the ratio of the useful energy to the total energy, where the leakage energy is considered a wasted energy.

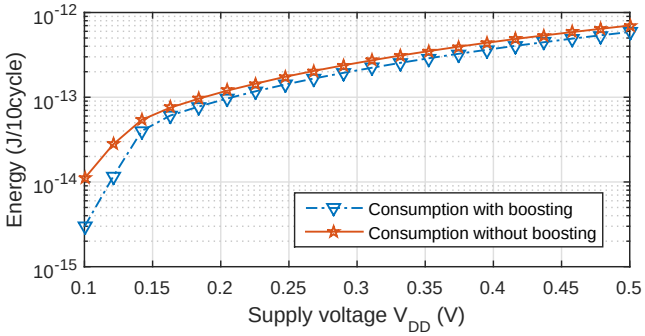

Fig. 5. Energy power consumption of buffers under scaling of supply voltage.

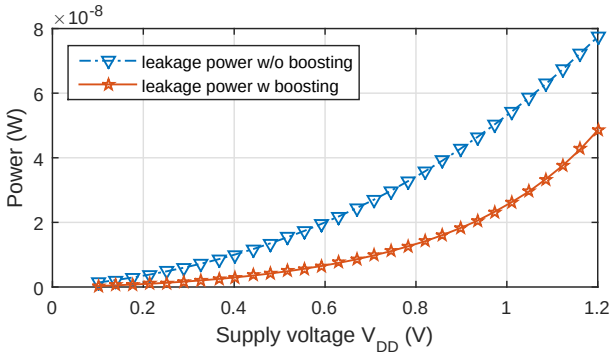

Fig. 6. Power leakage of the drivers.

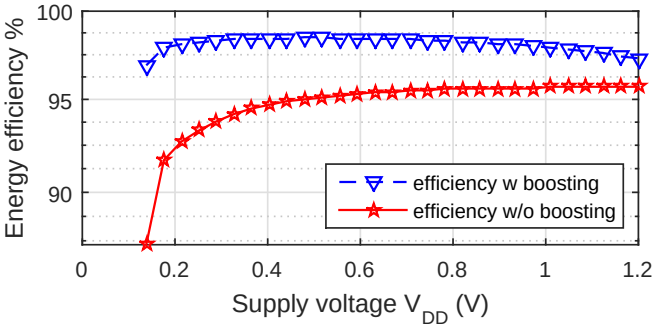

Fig. 7. Energy efficiency of the drivers.

IV. Conclusion

Interconnect drivers used in ultra-low power regime for clock distribution networks and on-chip buses suffer from considerable degradation in performance due to the fact that wire capacitance has not been scaled as the supply voltage is scaled down. Added to that, there is an issue of performance variability at sub-threshold region. So our approach has proposed using buffers with a charge pump booster, and this has met the expectations of improvements in performance by reducing power consumption and increasing energy efficiency. The reason for this is that the current driving is improved due to the exponential relationship between the transistor drain-to-source current and the gate-to-source voltage. The proposed driver shows an improvement in energy consumption which is 20% less than that of a conventional driver, and moreover the driver without boosting consumes 24% more power than our driver which shows improvements compared to other previously reported boosted drivers as well.

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