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A Smart All-Digital Charge to Digital Converter.

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A Smart All-Digital Charge to Digital Converter

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***Abstract*—Capacitance sensors, that report the values of capacitances as digital codes, are important in such areas as biomedical, environmental, and mobile applications. Voltage sensors are also widely used in many modern application areas, e.g. where battery life information is important. Conventional capacitance sensing methods use complex ADC techniques that are power hungry, and existing digital solutions, which use the charge to digital conversion (CDC) method tend to suffer from slow sensing response. A novel dual-use all-digital CDC method is proposed in this paper, which can be used to sense either capacitance values as a capacitance sensor or voltage levels as a voltage sensor. It shows low power/energy consumption and fast sensing response.**

I. INTRODUCTION

In such modern application areas as biomedical, environmental and mobile systems, the sensor is an essential device. Low-power and fast response are the two most important features of sensors used in such areas, particularly in terms of body monitoring and implants [9][10][12]. One of the main types of sensors detects capacitance values, which can be used to measure various physical quantities, including position, pressure, concentration of certain chemicals, etc. This is based on the fact that these physical quantities may be made to charge a capacitor so that this charge reflects the value of the parameter [8]. Typical capacitance sensors use charge sharing or charge transferring between capacitors to convert the sampled capacitance to voltage. This approach requires complex analogue circuits, such as amplifiers and ADCs, which increase design complexities and often increase power consumption [7]. Integrating capacitive sensors into many applications including wearable/implantable wireless sensor systems is therefore challenging due to the total system power/energy budget, which can be in the range of a few *nW* [1][2][3][4][5].

Similar to capacitance, voltage level is also an important parameter to be sensed in many applications. For example, in Energy Harvesting (EH) systems, voltage levels are monitored during energy accumulation. Based on the different voltage levels, different tuning mechanisms are used to achieve greater energy accumulation efficiency [14][15].

This paper proposes a novel versatile method that not only can be used to sense capacitances but also can be used to sense voltages by using fully digital solutions based on iterative delay chain discharge. Important characteristics including system complexity, measurement time, and power/energy are better than existing solutions.

In this paper, Section II presents the theory of capacitance to digital methods. Section III presents the implementation details. Section IV gives experimental results and Section V concludes the paper and discusses future work.

II. GENERAL THEORY OF DIGITAL DISCHARGE CDCS

Figure 1 shows the iterative delay chain discharge method. A Capacitance C_{sense} is charged to an initial voltage level V_{high} and then discharged to a pre-defined reference voltage level V_{low}. The number of iterations of discharging is then calculated and it is related to the initial voltage level V_{high} and the value of C_{sense}.

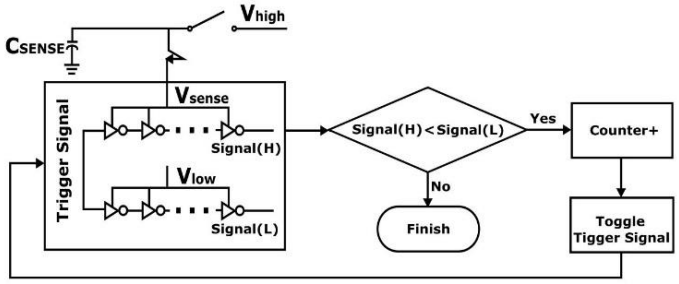

Figure 1. Iterative delay chain discharge method

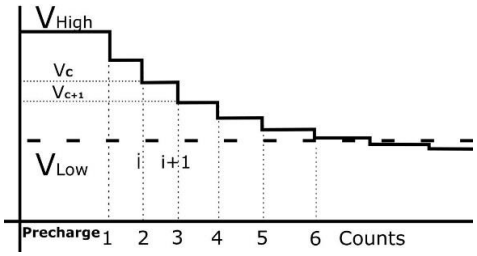

Figure 2. Discharge process.

Specifically, the voltage across C_{sense}, V_{sense}, is initially charged to V_{high}. C_{sense} will then be discharged due to the upper inverter chain powered by V_{sense}. As the two inverter chains are powered by V_{sense} and V_{low} respectively, the relationship of the delays of the two inverter chains is closely linked to the relationship of V_{sense} and V_{low}. The higher the supply voltage is, the smaller the delay it generates. So, the delay of the upper inverter chain will be compared with the delay of the lower inverter chain. Initially V_{sense} is higher than V_{low}, and the upper inverter chain has a shorter delay. When V_{sense} is discharged to V_{low}, the delays become the same. In other words, if $Signal_{(H)}$

comes earlier than $Signal_{(L)}$, it means V_{sense} is greater than V_{low}. As a result, more discharging is required. The counter is incremented by 1, the trigger signal is toggled, and another iteration of discharge will be performed. Otherwise, V_{sense} has been discharged to V_{low}. The iterations stop, and the value of the counter is used to represent the value of V_{high} / C_{sense} and hence the physical parameter being measured. The Mathematical theory of sensing capacitance and voltage is shown below.

A. Sensing Capacitance

Figure 2 shows the capacitance to digital discharge process. At step i, $Q_i = C_{sense}*V_i + C_p*V_i$, and at step i+1 $Q_{i+1} = C_{sense}*V_{i+1} + C_p*V_{i+1}$ where C_p is the capacitance of the circuit onto which the charge on C_{sense} is discharged, i.e. the upper inverter chain. In between steps i and i+1, the discrete view (Figure 2) is that the charge on C_p is depleted through the circuit to 0. As a result, $C_{sense}*V_i = (C_{sense}+C_p)*V_{i+1}$, and we can derive the following formula:

$$\frac{V_{i+1}}{V_i} = \frac{C_{sense}}{C_{sense}+C_p} \quad (1)$$

and assume $V_{i+1} = V_i*(1-k)$, then

$$k = \frac{C_p}{C_{sense}+C_p} \quad (2)$$

We can then model the discharge process by using the equation:

$$V_{low} = V_{high}(1-k)^n \quad (3)$$

where n is the number of steps taken to discharge V_{sense} from V_{high} to V_{low}.

Based on the Taylor series,

$$(1-k)^n = 1 - nk + \frac{n(n-1)k^2}{2!} - \frac{n(n-1)(n-2)k^3}{3!} + \cdots$$

and, if nk<<1, the above formula can be approximated as:

$$(1-k)^n = 1 - nk \quad (4)$$

From (3), if we have V_{high} and V_{low} fixed (i.e. *const*) by the measurement method, we must have $(1-k)^n$=*const*. Thus, under nk<<1, we have 1-nk=*const* and thus nk=*const*, and hence

$$n\frac{C_p}{C_{sense}+C_p} = const \quad (5)$$

So, if C_{sense}>>C_p, then $C_{sense}+C_p \approx C_{sense}$. We will have

$$n\frac{C_p}{C_{sense}} = const \quad (6)$$

and thus n must be linearly proportional to C_{sense} with fixed V_{high} and V_{low}. This means that with fixed V_{high}, and V_{low}, the value of n can be used to derive the value of a tested capacitor.

B. Sensing Voltage

The discharging process in the distinctive super-threshold region, under the assumption of α=2, was derived according a geometric series sum technique in [13].

$$V_{low} = V_{high}K^n \quad (7)$$

Where $K = \frac{C_{sense}}{C_{sense}+C_p}$

here $K = 1 - k$

With constant V_{high} and V_{low}, the discharge process determines the value of C_{sense}. Similarly, if C_{sense} is fixed, it can be used to determine V_{high}. After n steps, V_{high} is discharged to V_{low}, then based on equation (7), we finally have,

$$n = \log_K(\frac{V_{low}}{V_{high}}) = -\log_K(\frac{V_{high}}{V_{low}}) \quad (8)$$

As a result, n is logarithmic with the sensed voltage (V_{high}). This means that with a fixed capacitor and a fixed V_{low}, n can be used to derive V_{high} to form a voltage sensor.

III. Design Implementation

Figure 3 shows the proposed design in asynchronous circuits [6] to achieve the sensing functions. The implementation includes 4 blocks: signal generator, event generator, event comparator and event counting mechanism. The upper inverter chain is powered by V_{sense} and the other components are powered by V_{low} to save power. After C_{sense} is fully charged, the switch turns off, and then the sensing mechanism is started. A *Clk* signal is generated to trigger the event generator. The event generator (two inverter chains) then generates two events with different delays when V_{sense} and V_{low} are different. These events are then compared in the event comparator to determine which one comes earlier. If the event from bottom inverter chain comes earlier, the sensing mechanism will be stopped. Otherwise, a new *Clk* signal is generated for the next round. The *Clk* signal then goes through a level shifter to the appropriate voltage (V_{sense}) as an input to the event generator's upper inverter chain to repeat the steps again until V_{sense} drops to below V_{low}. Eventually, the event counter outputs the number of transitions of the *Clk* signal. The number of transitions, or the output code, is related to the capacitance of the sensed capacitor under fixed voltage level or the sensed voltage level under a fixed capacitance.

The function of the MUTEX block is to ensure that metastability, if it happens, does not propagate outside the event comparator. If the two events being compared occur close to each other, metastability may happen at the comparator and the MUTEX may take some time to decide which event 'wins' the comparison. The comparator does not issue a valid result until it has resolved any metastability inside, making sure that its output signal can only take the values of logical 0 or 1 securely and no nondeterministic middle value can be sent out. In other words, the value of the comparison is always correct with or without metastability, which could only cause a non-deterministic delay in the worst case. This delay is tolerable as the entire sensing system is asynchronous and metastability settling time is usually very short.

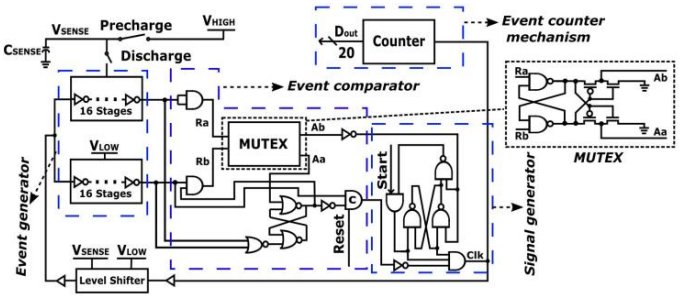

Figure 3. Asynchronous Implementation.

IV. EXPERIMENTAL RESULTS

Our design has been implemented in UMC 90nm CMOS technology. Figure 4 shows a simulation result of our design. V_{high} is set to 1V, which means that V_{sense} is 1V at the beginning, V_{low} is set to 0.45V and C_{sense}=50pF. Here this first experiment is only used to show the concept of the proposed mechanism. For sensing purpose, only one of V_{high} and C_{sense} will be fixed.

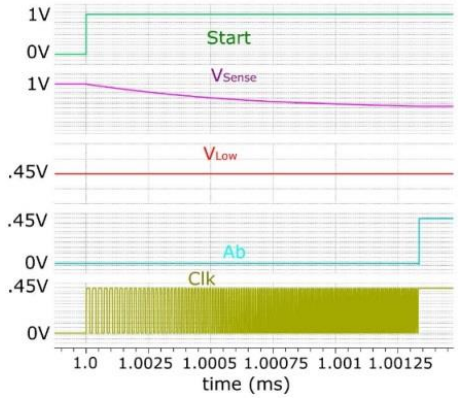

Figure 4. Simulation results.

The rising of the ***Start*** signal triggers the discharging of V_{sense} and the *Clk* signal starts to be generated. When V_{sense} drops to V_{low}, the delay of the inverter chain powered by V_{sense} catches up with the delay of the other inverter chain powered by V_{low}. After that, A_b will be generated to high and the *Clk* stops oscillation. Then the 20-bit counter calculates the total amount of *Clk* rising signals, when $V_{sense} > V_{low}$.

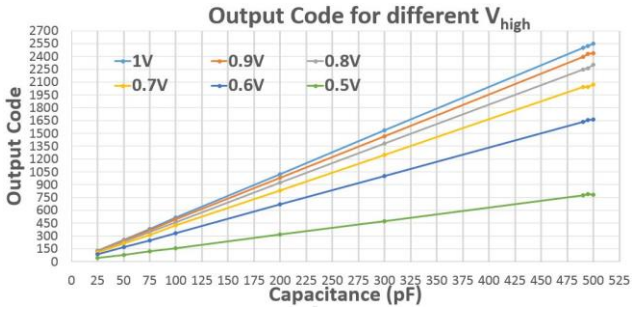

Figure 5. Output codes for different V_{high}

After this initial demonstration, experiments have been done to characterize the design as a capacitance sensor as shown in Figure 5. Here, different V_{high} values are used from 0.5V to 1V, shown in different colors in the figure, and V_{low} is set to 0.45V. These experiments produced a relationship between the output code and C_{sense} given any valid V_{high} value. For example, set V_{high}=0.8V, with V_{low}=0.45V. If output code = 232, then we can say that C_{sense} = 50pF and if output code = 2306, then we can derive that C_{sense} = 500pF. As can be seen from Figure 5, the output codes under the same V_{high} for different capacitance values are linear. The results agree with the theory in Section II.A. For each value of V_{high}, we can determine a specific formula for the output code to C_{sense} relationship. This means that for a fixed V_{low}, if we know the output codes and V_{high}, we will be able to calculate the value of the capacitance. The value of V_{high} can be used to tune the sensing precision vs. speed and energy tradeoff. The higher V_{high} is, the higher the sensing precision is, at the cost of longer sensing time and greater sensing energy consumption. This is because for the same C_{sense}, charging to a higher voltage needs more energy and leads to the discharging process taking longer.

Figure 6 shows the third group of experiments to characterize the design as a voltage sensor. Here several fixed values of capacitors are used. For example, in Figure 6, different colors of lines represent different C_{sense} values, from 25pF to 500pF. V_{low} is set to 0.45V again. When setting C_{sense} = 500pF, with V_{low}=0.45V, if output code = 1664, then we can find that V_{high} = 0.6V and if output code = 2306, then we can derive that V_{high} = 0.8V. As can be seen from Figure 6, with any fixed C_{sense} value, the output codes have a logarithmic relationship with V_{high} values. These results confirm the theory in Section II.B. For each value of C_{sense}, we can determine the specific formula for the relationship between output code and V_{high}. Then, if we know the output codes and V_{low}, we will be able to calculate V_{high}, similar to when the design is used for capacitance sensing. Also similarly, the value of C_{sense} can be used to tune the sensing precision vs. response time and energy tradeoff. The higher of the value of the fixed C_{sense}, the higher the precision of the measurement is, at the cost of longer sensing time and greater sensing energy. This is because using the same V_{high} to charge a larger C_{sense} takes greater energy, leading to a longer discharging process.

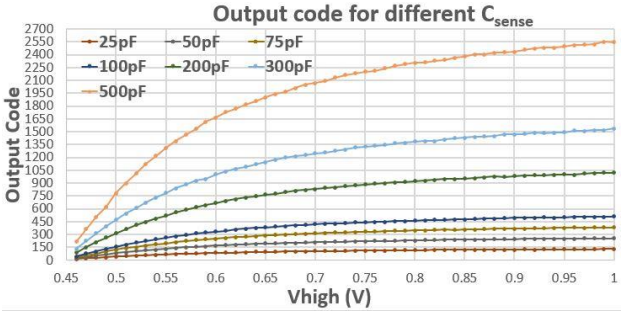

Figure 6. Output codes for different C_{sense}

The characterization experiments demonstrated the viability of this design for its two intended uses. Next this design is compared with existing work for performance metrics including response time, average power and energy per sensing round. Table 1 shows the comparison of these performance metrics in an example operation case with V_{sense} discharging down from V_{high}=1V to V_{low}=0.45V with C_{sense}=50pF. As can be seen, the response time, power consumption and energy consumption per sense round decrease 12.8%, 24.7% and 32.65% respectively.

Table 1. Comparison results when V_{high}=1V,V_{low}=0.45V & C_{sense}=50pF

	[7]	This Work	Difference
Response Time	1.084us	0.945us	12.8%
Power	26.039uW	19.611uW	24.7%
Energy	28.663pJ	19.329pJ	32.65%

Given the target of biomedical, environmental and mobile applications, the complexity of the solution is also an important metric. In general, the fewer transistors used, the lower the system unit price, and the faster a system will

perform consuming less power and energy. Table 2 shows the comparison in terms of the number of gates and flip-flops used between this work and [7]. In total, the design in [7] used 258 gates and 52 flip-flops. In this work, the circuits contain 107 gates, which is 59% fewer and 20 flip-flops, which is 62% fewer.

The snapshot of an ASIC chip of the proposed design is shown in Figure 7. The top area is the main circuit including signal generator, event generator and event comparator, the middle area is a 50pF capacitance used for on-chip testing and the bottom area is the 20 bits counter. It was designed in UMC 90nm CMOS technology. The size of the layout is $0.0015mm^2$ (23.2µm*65µm).

Table 2. Implementation size comparison

	No. of gates in [7]			No. of gates in this work			Diff.
	core	counter	total	core	counter	total	
Inv.	63	104	167	43	19	62	63%
Buf.	4	0	4	2	0	2	50%
P. Trans	2	0	2	2	0	2	0
Trans G	1	0	1	1	0	1	0
NAND2	25	52	77	17	19	36	53%
NAND3	4	0	4	2	0	2	50%
LS	3	0	3	1	0	1	66%
DFF	0	52	52	0	20	20	62%
Total			310			126	59%

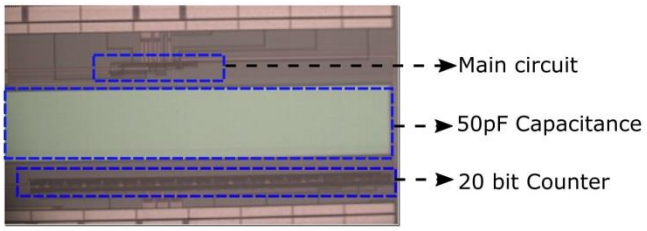

Figure 7. Snapshot of the chip

V. CONCLUSIONS AND THE FUTURE WORK

This paper presents the general theory of capacitance/voltage to digital conversion through discharging for sensing both capacitance and voltage. An asynchronous solution is systematically designed, and implemented in UMC 90nm CMOS technology. The proposed method and design shows application diversity as it can be used to sense not only capacitance but also voltage. As a capacitance sensor it achieves linearity between the output codes and the sensed capacitance value. As a voltage sensor the output codes are related to the sensed voltage value logarithmically, which displays a variable precision across the sensing voltage range.

The performance of this design is better in terms of the important metrics energy/power consumption and response time than the most recent existing CDC of a similar type, between 12.8% and 32.65% in one example operation scenario.

This degree of improvement is expected to be available across all operation scenarios as this design is considerably less complex than existing designs. For instance, it uses fewer than half of the number of gates compared with the most resent existing CDC of a similar type.

Experiments have confirmed the intuition that a greater value of V_{high} provides for higher capacitance sensing precision at the cost of longer sense response and higher sense energy consumption, and a greater value of C_{sense} provides for higher voltage sense precision, also at the cost of longer sense time and higher sense energy consumption.

The chip has been taped out. Hardware measurement tests are planned with the help of an on-chip 50pF capacitance and off-chip capacitors of different values.

The hardware test results will then be compared to the reported simulation results. These test results are expected to become available before the expected date of the conference.

VI. ACKNOWLEGEMENT

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