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Link to paper:


Date deposited:

08/11/2017
Multiphase Ternary Fibonacci
2D Switched Capacitor Converters

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Abstract—The paper proposes a method to use the Fibonacci numbers with odd and even indices for synthesis of switched capacitor converters (SCCs) with multiphase control. As in the previously developed method using high-radix positional numeral systems, the capacitors in the proposed method can be connected in parallel. For this purpose, a special two-dimensional (2D) array of switches is introduced. Thus, all the available earlier target voltages as well as those defined by the Fibonacci numbers with odd and even indices, can be obtained using the same array of switches. Owing to small distance between the neighboring target voltages, the total SCC efficiency can be increased. The theoretical results were verified by simulations.

Keywords—Charge pump, efficiency, signed-digit number system, switched capacitor converter, topology.

I. INTRODUCTION

Switched capacitor converters (SCCs) are favored in some applications due to low EMI and compatibility with integrated circuit technology. It is known that SCCs exhibit high efficiency only when their output voltage, \( V_o \), is close to the target voltage, \( V_{TRG} = MV_{in} \), where \( M \) is the no-load conversion ratio. When a SCC is loaded, the capacitors are cyclically recharged by the current through the switches. This current defines the so-called conduction losses [1], [2], which are modeled by an equivalent resistance, \( R_{eq} \), as shown in Fig. 1. Thus, a high efficiency is provided only in the case if \( R_{eq} \) value is small. To regulate \( V_o \), one can adjust \( R_{eq} \), while \( M \) takes only discrete values.

The name “multiphase SCCs” presumely that these converters have a large number of degrees of freedom. The idea of this paper is to use the available degrees of freedom to increase the total SCC efficiency. Architecturally, the multiphase SCCs can be divided into two classes. In the first one, the flying capacitors are always connected in series by a one-dimensional (1D) array of switches. The 1D class is represented by two different binary SCCs [3], [4] and the generalized Fibonacci SCC [5]. In the second class, groups of the flying capacitors or the capacitors themselves are connected in series and in parallel. All the necessary connections are provided by a two-dimensional (2D) array of switches. Note that some combinations available in a 1D array can not be available in a 2D array.

The 2D class is represented by the Capacitive Transposed Series-Parallel (GTSP) topology [6], the so-called GFN based SCCs [3], [7] and the binary-ternary SCC [8]. It should be noted that for the GFN based SCCs a special 2D array of switches has never designed. Theoretically, 4 flying capacitors in this SCC allow obtaining 17 different conversions ratios. Thus, the total efficiency will have 17 peaks as shown by solid line in Fig. 2. The objective of this paper is to introduce additional conversion ratios to the GFN based SCC. To this end a new signed-digit number system with high redundancy is used. The dashed line in Fig. 2 shows the additional peaks of efficiency. It should be noted that some conversion ratios can be obtained in different ways and therefore the same peak may have different height.

II. SIGNED TERNARY FIBONACCI (STF) REPRESENTATIONS

For the initial values \( F_{-1} = 1 \) and \( F_0 = 0 \) the Fibonacci numbers are defined as:

\[
F_i = F_{i-1} + F_{i-2}
\]

First eight Fibonacci numbers are given in Table I.

<table>
<thead>
<tr>
<th>( i )</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
<th>6</th>
<th>7</th>
<th>8</th>
</tr>
</thead>
<tbody>
<tr>
<td>( F_i )</td>
<td>1</td>
<td>1</td>
<td>2</td>
<td>3</td>
<td>5</td>
<td>8</td>
<td>13</td>
<td>21</td>
</tr>
</tbody>
</table>

Let us denote by \( \alpha \) and \( \beta \) the cases when only odd or only even indices are used. Any natural number \( N_n^\alpha \in [0, F_{2n-1}] \) or \( N_n^\beta \in [0, F_{2n}] \) with a resolution \( n \) can be represented as a sum of the Fibonacci numbers:

\[
N_n^\alpha = \sum_{j=1}^{n} A_j F_{2(n-j)+1}
\]

\[
N_n^\beta = \sum_{j=1}^{n} A_j F_{2(n-j)+2}
\]

where \( A_j \in \{0,1,2\} \). It has been shown in [9], [10] that the representations (2) and (3) are unique if any two consecutive 2s are separated by at least one 0. Each of these representations is referred hereinafter to as “original code”. For \( n = 1,2 \) the original codes of \( N_n^\alpha = 1 \ldots 5 \) and \( N_n^\beta = 1 \ldots 8 \) are given in Table II.

---

Fig. 1: The equivalent circuit of a SCC.

Fig. 2: The expected total efficiency of the proposed SCC.
Let us consider an addition of two digits in the original code. Substituting \( k = i + 1 \) into (1), we can write:

\[
F_k = F_{k+2} - F_{k+1} \quad \text{and} \quad 2F_k = F_{k+1} + F_{k-2}
\]  

Summing these two expressions, we obtain:

\[
3F_k = F_{k+2} + F_{k-2} \quad \text{and} \quad 4F_k = F_{k+2} + F_k + F_{k-2}
\]

The indices \( k \pm 2 \) in the case that means that adding 2 to \( A_j > 0 \) gives two carries, one position to the left and to the right. For \( A_j = 1 \) the sum is equal to 0, and for \( A_j = 2 \) it is 1.

For a resolution \( n \) we define Signed Ternary Fibonacci (STF) representations for fractions \( M_n^0 \in [0,1] \) and \( M_n^0 \in [0,1] \) as:

\[
M_n^0 = A_0 + \sum_{j=1}^{n} A_j \frac{F_{2(n-j)+1}}{F_{2n+1}}
\]  

\[
M_n^0 = A_0 + \sum_{j=1}^{n} A_j \frac{F_{2(n-j)+2}}{F_{2n+2}}
\]

where \( A_0 \in \{0,1\} \) and \( A_j \in \{0, \pm 1, \pm 2\} \). Since \( A_j \) takes the negative values, both of the STF representations have high redundancy. The original codes for \( M_n^0 \) and \( M_n^0 \) correspond to those for \( N_n^0 \) and \( N_n^0 \). Considering this correspondence, we will write hereinafter just “original code” of \( M \).

**Rule for spawning the STF codes:** Add 2 to any \( A_j > 0 \) in the original code of \( M \geq 1/2 \). This will give either 0 or 1 and two carries. To keep the value of \( M \), subtract 2 from the obtained \( A_j \) and spawn thereby a new STF code. The above procedure repeats for all \( A_j > 0 \) in the original code and for all \( A_j > 0 \) in each new STF code. For the complementing fraction, \( 1 - M \), multiply all the obtained STF codes of \( M \) by \(-1\) and add 1 to every \( A_0 \).

**Corollary 1:** For a resolution \( n \), the minimum number of STF codes is \( n+1 \). This is because each \( A_j > 0 \) in the original code gives a new STF code and two carries. These carries propagate, such that each 0 in the original code is turned to \( A_j > 0 \), which is also operated on to spawn a new STF code.

**Corollary 2:** Each \( A_j > 0 \) in the STF code gives at least one \( A_j < 0 \) in the same position \( j \) of another STF code. This is because the spawning rule involves subtracting 2 from \( A_j < 2 \).

Fig. 3 shows how the first STF code for \( M_2^0 = 4/5 \) and for \( M_2^0 = 7/8 \) is spawned from the corresponding original code. Since \( F_{-1} = F_1 = 1 \), the LSB overflow in the case of odd indices \( M_n^0 \) means that we just need to add 1 to the LSB digit.

In the case of even indices \( M_n^0 \) this overflow is disregarded, since \( F_0 = 0 \). For \( n = 1 \) the STF codes are given in Table III and coincide with the corresponding GFN codes.

![Table II: Original codes for \( N = 1 \ldots 8 \).](image)

![Table III: The STF codes for \( M_1^0 \) and \( M_2^0 \).](image)

For \( n = 2 \) the STF codes are given separately for the case of odd and even indices in Table IV and Table V respectively.

**III. TRANSLATING STF CODES TO SCC TOPOLOGIES**

The rules for translation the STF codes to SCC topologies are a particular case of the corresponding rules for the GFN based SCCs [3, 7]. Let us have a voltage source \( V_{in} \), a set of \( 2n \) flying capacitors and an output capacitor, \( C_o \), connected in parallel with a load \( R_o \). The flying capacitors are divided into \( n \) groups of two capacitors \( C_{j1} \) and \( C_{j2} \) in each group \( j \). For a given \( M \), the interconnections of \( V_{in}, C_{j1,2} \) and \( C_o \) are carried out according to the following rules:

1) If \( A_0 = 1 \) then \( V_{in} \) is connected.
2) If \( A_0 = 0 \) then \( V_{in} \) is disconnected.
3) If \( A_j = -2 \) then \( C_{j1} \) and \( C_{j2} \) are connected in series with the same polarity and charged.
4) If \( A_j = -1 \) then \( C_{j1} \) and \( C_{j2} \) are connected in parallel and charged.
5) If \( A_j = 0 \) then \( C_{j1} \) and \( C_{j2} \) are disconnected.
6) If \( A_j = 1 \) then \( C_{j1} \) and \( C_{j2} \) are connected in parallel and discharged.
7) If \( A_j = 2 \) then \( C_{j1} \) and \( C_{j2} \) are connected in series with the same polarity and discharged.

Let us assume that in steady-state all the capacitors in the SCC topologies of Fig. 4 are charged to constant, but unknown voltages \( V_1 = V_{1,1} = V_{1,2}, V_2 = V_{2,1} = V_{2,2} \) and \( V_o \).

![Table V: The STF codes for all the conversion ratios \( M_n^0 \).](image)
To find these voltages we apply Kirchhoff’s Voltage Law (KVL) to each topology, which leads to the following system of four linear equations:

\[
\begin{pmatrix}
1 & 2 & -1 \\
2 & 0 & -1 \\
-1 & 1 & -1 \\
0 & -1 & -1 \\
\end{pmatrix}
\begin{pmatrix}
V_1 \\
V_2 \\
V_3 \\
V_4 \\
\end{pmatrix}
= 
\begin{pmatrix}
0 \\
0 \\
0 \\
0 \\
\end{pmatrix}
\]

Solving this system, we obtain: $V_1 = \left(\frac{1}{8}\right)V_{in}$, $V_2 = \left(\frac{3}{8}\right)V_{in}$, $V_o = \left(\frac{5}{8}\right)V_{in}$. It is evident that (8) is over determined. We can eliminate the redundant equations and rewrite (8) as:

\[
\begin{pmatrix}
1 & 0 & 1 & 1 & -1 \\
-1 & 1 & 0 & 0 & 0 \\
0 & 1 & 0 & 1 & -1 \\
0 & 0 & -1 & 0 & -1 \\
\end{pmatrix}
\begin{pmatrix}
V_{1,1} \\
V_{1,2} \\
V_{2,1} \\
V_{2,2} \\
\end{pmatrix}
= 
\begin{pmatrix}
0 \\
0 \\
0 \\
-1 \\
\end{pmatrix}
\]

Strictly speaking, it is necessary to prove that for any resolution $n$ the KVL system composed of the SFT codes has a unique solution. Corollaries 1 and 2 are just a step towards this proof.

**IV. TWO-DIMENSIONAL (2D) ARRAY OF SWITCHES**

In the topologies of the ternary Fibonacci SCC each group of the capacitors needs to change the connection polarity or be disconnected $\{0, \pm 1\}$. In turn, the capacitors within each group need to have two types of connections $\{1, 2\}$. The 1D array of switches considered in [3], [5], [7], [11] provides all the above connections and is shown in Fig. 5. The disadvantages of this array are that the capacitors cannot be connected directly to the input and output and cannot be connected directly one to each other. Let all the switches in Fig. 5 have the same on-resistance, then topology © in Fig. 4 will look as shown in Fig. 6.

**V. SIMULATION RESULTS**

The proposed SCC has been simulated in PSIM 9.1 using the 2D array shown in Fig. 7. It comprises 32 bidirectional switches with an on-resistance of 1.2Ω. Each $C_{i,1,2} = 4.7\mu F$, $V_{in} = 8V$, and the time slot allotted for each topology $t = 5\mu s$. Since $R_{eq}$ is defined for the average (DC) output current, $I_{av}$, it is evident from the SCC equivalent circuit in Fig. 1 that

\[
R_{eq} = \frac{MV_{in} - V_o}{I_{av}} \quad \text{and} \quad \eta = \frac{R_o}{R_{eq} + R_o}
\]

To measure $I_{av}$, we use the examination circuit presented in Fig. 9, where $V_o = 0.95MV_{in}$. First the SCC reaches steady state, and then $I_{av}$ is read. The efficiency, $\eta$, was calculated for $R_o = 100\Omega$. The values of $R_{eq}$ and $\eta$ are given in Table VI.
The steady-state output current, $I_{o}$, is presented in Fig. 10 for $M_{o}^{2} = 4/5$ and in Fig. 11 for $M_{o}^{1} = 1/2$ and $M_{o}^{2} = 4/8$.

Table VI: Measured and calculated parameters.

<table>
<thead>
<tr>
<th>$M$</th>
<th>$I_{o}$, mA</th>
<th>$R_{eq}$, $\Omega$</th>
<th>$\eta$, %</th>
</tr>
</thead>
<tbody>
<tr>
<td>$1/8$, $3/8$</td>
<td>153.25</td>
<td>2.284</td>
<td>97.77</td>
</tr>
<tr>
<td>$1/5$, $3/5$</td>
<td>144.81</td>
<td>2.210</td>
<td>97.84</td>
</tr>
<tr>
<td>$1/4$, $3/4$</td>
<td>120.36</td>
<td>2.493</td>
<td>97.57</td>
</tr>
<tr>
<td>$1/3$, $3/3$</td>
<td>170.29</td>
<td>1.566</td>
<td>98.46</td>
</tr>
<tr>
<td>$3/8$, $5/8$</td>
<td>109.39</td>
<td>2.287</td>
<td>97.76</td>
</tr>
<tr>
<td>$2/5$, $3/5$</td>
<td>104.93</td>
<td>2.287</td>
<td>97.76</td>
</tr>
<tr>
<td>$2/3$, $5/3$</td>
<td>69.886</td>
<td>2.802</td>
<td>97.22</td>
</tr>
<tr>
<td>$1/2$</td>
<td>195.15</td>
<td>1.025</td>
<td>98.99</td>
</tr>
</tbody>
</table>

Fig. 9: Examination circuit for the SCC.

VI. CONCLUSIONS

Based on the numeral systems using the Fibonacci numbers with odd and even indices, two new STF representations have been proposed. The fact that these representations are redundant means that the SCC control needs to be multiphase. To obtain the STF codes, an iterative rule is used. The corollaries of this rule provide necessary (but not sufficient) condition for correct operation of the proposed SCCs. To increase the output current, the 2D array of switches has been developed. This array can also be used to obtain the conversion ratios available in the GFN based SCCs. In case if the 1D class of SCCs is not considered, the proposed SCC with 4 flying capacitors allows one to obtain 22 conversion ratios. Among them 17 are available, but have never been realized in the GFN based SCC. These 17 conversion ratios include 7 that have been obtained using the proposed method. Additional 4 conversion ratios, namely $\{1/8, 3/8, 5/8, 7/8\}$, were first introduced in this paper.

The efficiency of the proposed SCC in the simulations for each conversion ratio at $R_{eq} = 1000 \Omega$ is above 97%. As evident from Table VI and Fig. 11, for the same $M_{o}^{1} = M_{o}^{2} = 1/2$ we have different values of $R_{eq}$ and different form of the output voltage ripple. This feature is useful if one needs to regulate $V_{o}$ in the intervals between the conversion ratios. In general case, the regulation is done by frequency or/and duty cycle control, but at the expense of increased losses and consequently, a lower efficiency. The ripple of the output current can be reduced by switching the topologies forward and backward [11]. It would be interesting to realize the 2D array of switches on-chip, that is to develop further the idea of field programmable array [12]. The proposed SCCs can be considered as an analog computer that uses an iterative method to solve the systems of linear equations.

ACKNOWLEDGMENT

This research was partly supported by EPSRC, grants SAVVIE (EP/K012908/1) and A4A (EP/L025507/1).

REFERENCES