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Pulse Controlled Memristor-based Delay Element

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***Abstract*—Computing circuits suffer from the process, voltage and temperature variations and aging. These factors reduce yield and lifetime of the circuits and therefore limit the advance in modern computing technology. The process variations and aging result in timing failures that often can be resolved by delay matching. However, this strategy requires delay elements which cause additional power cost. We propose an alternative approach to implementing a pulse controlled delay element using a novel "memristor" device. The delay element has three modes of operation: tune up, tune down and normal. The main advantage of this approach is the energy efficiency due to the absence of the current path in the normal mode. Furthermore, as memristor is a non-volatile device, the proposed delay element does not need to be re-initialized every time the system starts. Thus, it can save startup power and time, which is also critical in the beyond CMOS computing. We also identify and propose a solution to the backward tuning problem which occurs when the amplitude of the normal signal is higher than the memristor threshold. A prototype was built based on ferroelectric parameter set with VTEAM model and the high voltage AMS 0.35μm technology. The simulation results showed an effective delay range from 5.48ns to 13.54ns in 6 steps with the minimum tuning pulse width of 3ns and the average delay of 1.34ns per step.**

***Keywords*—memristor, delay element, pulse control**

I. Introduction

In 1971, Leon Chua originally introduced a memristor, which is a 2-terminal device, to replace a missing link between charge (q) and flux (φ) [1]. The name memristor is a combination of "memory" and "resistor" which is its unique characteristic where its internal resistance called "memristance" can be changed by applying current or voltage across its terminals, and this state is still permanent even when the power is removed. In 2008, the first practical device was invented by HP lab [2]. It was composed of two thin-layer TiO_2 films, one with oxygen vacancies, between two terminals. The applied power forces the oxygen vacancies toward the adjacent layer thus reduces the memristance; these vacancies move back when the opposite power is applied.

The memristor is considered a novel computing and memory device because of its exceptional properties such as non-volatility, fast switching, small area, low energy dissipation and compatibility with the CMOS process [3] [4] [5]. Furthermore, it has a high endurance of 10^{12} cycles [6] which is better than NAND Flash and close to DRAM and SRAM ($> 10^{16}$ cycles) [7]. Additionally, its data retention is very long – 10 years [6] [8]. Due to these benefits the research on memristor is expanding from memory to many other domains, such as neural networks, neuromorphic system and computation circuit [3] [8].

As the technology scaling is being limited by the process, voltage, and temperature (PVT) variations, the tunable delay elements play a crucial role in variation tolerant design techniques, such as post-fabrication delay tuning [9] [10]. Furthermore, the circuit aging that causes timing violations in the long term, can be also addressed by self-healing techniques using tunable delays [11]. These techniques are also applicable to mitigating the timing errors in the bundled data asynchronous pipelines [12].

There are many approaches to the design of reconfigurable delay elements. [13] and [14] proposed current starved inverter-based delay elements whose delays are highly dependent on the transistor sizes. Therefore they are susceptible to process variation. Moreover, a current mirror in [14] results in constant drain of current and static power consumption. A simple yet effective multiplexer-based inverter-chained delay element was introduced in [15]. However, a significant amount of power is spent by a large transistor count. In [16] a linear comparator-based design is proposed which, however, is difficult to couple with digital circuits and prone to the voltage variation due to the need of an analog signal for configuring the delay. Several proposals to use memristor for delay elements have their own limitations. For example, the design in [17] can provide the delay for one transition only, while the design in [18] is risky due to the backward tuning problem, as discussed in Section III-C.

Overall, the demand for the tunable delay elements has increased as the PVT variations and the effects of aging become more severe. Therefore, resolving the existing issues with reconfigurable delays is vitally important and we believe the memristor is a key component to do the job. By placing it between two simple CMOS inverters one can form a high resistance wire. This circuit can produce delay on both rising and falling transitions, yet eliminating the power consumption, tolerating PVT variations, and supporting a digital interface for tuning. Based on non-volatile feature, the delay value is preserved in the memristor even when the power is off, thus there is no need for an additional storage element. This helps to reduce the overheads for the power, time and memory space that otherwise would be inevitable for keeping and retrieving every delay value in the system. The memristor circuit also enables support for delay variation and aging tolerant system by the pulse-based runtime tuning feature which allows the delay to be adapted to the specific circumstances.

In the circuit design, we rely on the Voltage ThrEshold Adaptive Memristor (VTEAM) model [19]. It is a threshold-based voltage-driven model where the memristance changes only when the applied voltage is out of the threshold range. The flexibility of the VTEAM model enables its coupling with the other models and even with the extracted characteristics

of devices [20]. In the future this model can be extended to support the newly invented devices. To make sure the technical issues can be observed and a prototype circuit can be fabricated, the memristor model and its parameters are preserved in this work.

The main contributions of this paper are as follows:

- Design of a conceptual power-efficient memristor-based reconfigurable delay element with the untouched memristor model and parameters.
- Discovery of the backward tuning issue and development of a solution to this problem.
- Extensive characterization of the proposed delay element (the maximum effective memristance, maximum delay, minimum pulse width, number of step, average delay step and power consumption).
- Detailed comparison of the proposed design against existing solutions.

The rest of the paper is organized as follows: Section II introduces the memristance and the VTEAM models [19]. Design of the proposed memristor-based delay element is the subject of Section III. Experimental results are presented in Section IV and compared to the related works in Section V.

II. Background

In this section, the memristance and VTEAM models are described in details. The former model captures the relationship between the width of the doped region and the memristance which translates to a particular delay in the circuit. The latter model converts the applied voltage, excitation time and related parameters into the width of the doped region.

A. Memristance model

The memristance model introduced in [2] consists of doped and undoped regions, as illustrated in Fig. 1. The doped region contains oxygen vacancies which cause a low resistance, while the other region comprises a pure titanium dioxide that provides a high resistance. The undoped region width w can be changed by applying the current to move the vacancies to the other region – this cause a shift in the total memristance (R_m). Finally, when the vacancies reach the other end ($w = D$), the total memristance becomes R_{on}. In the opposite way, when all the vacancies are pushed back ($w = 0$), the total memristance becomes R_{off}. Therefore, the mathematical model is composed of these resistors connected in series and the state variable which is denotes the proportion of the doped region width $w(t)$ to the total width D as in (1).

$$R_m = R_{on}\frac{w(t)}{D} + R_{off}(1 - \frac{w(t)}{D}) \tag{1}$$

Equation (1) implies that the memristance only depends on the width of the doped region. Therefore, the delay tuning technique in this paper only relies on the width adjustment which is modeled in Section II-B. Notice that the "doped region width" is often referred to as the "state variable" in the literature, therefor we use this term for consistency.

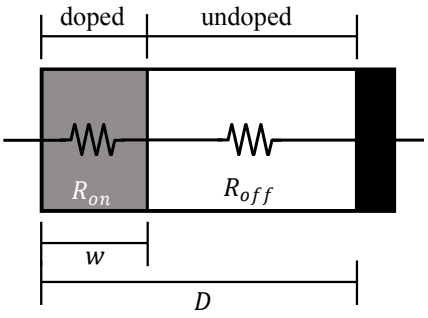


Fig. 1: Memristance model.

B. VTEAM model

Based on the threshold-based voltage-driven model, the memristance only shifts when the voltages across its terminals are greater than its v_{on} and v_{off} thresholds. As shown in Fig. 2, the VTEAM defined the v_{on} as the negative polarity while v_{off} as the positive one. The memristance turns to R_{on} when the voltage V_{pn} less than the v_{on} is applied. Contrary, it turns to R_{off} when V_{pn} is higher than v_{off}.

The model equation (2) indicates the factors that impact the change of the doped region width $dw(t)$ and, consequently, memristance and delay. These parameters are important in term of memristor properties and fabrication technology matching. To clarify, the thresholds define the minimum operating voltage that must not be less than $Max(|v_{on}|, |v_{off}|)$.

$$\frac{dw(t)}{dt} = \begin{cases} k_{off}(\frac{v(t)}{v_{off}} - 1)^{\alpha_{off}} f_{off}(w), & 0 < v_{off} < v \\ 0, & v_{on} < v < v_{off} \\ k_{on}(\frac{v(t)}{v_{on}} - 1)^{\alpha_{on}} f_{on}(w), & v < v_{on} < 0 \end{cases} \tag{2}$$

This voltage determines the tuning speed that also relates to the tuning duration dt and doped distance shift $dw(t)$. Table I summarizes memristor fitting parameters from [19] and [21] and provides examples of the total tuning time with different bias voltages which is useful in memristor selection, as discussed in Section III-C.

The VTEAM model is as efficient and accurate tool [20] for determining the appropriate supply voltages and memristor type that match the target technology while meeting the requirements for the switching speed and the memristance range. It is implemented in Verilog-A which makes it convenient for integrating with design tools [19].

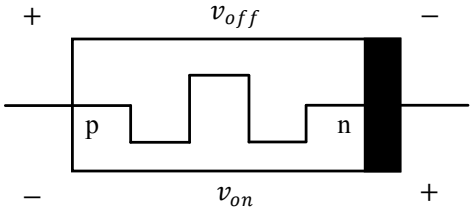


Fig. 2: Memristor symbol with voltage threshold notations.

TABLE I: Memristor Fitting Parameters for VTEAM.

Parameter	Ferroelectric [19]	BCM [19]	MAGIC [21]
α_{off}	5	1	4
α_{on}	5	1	4
v_{off} (V)	1.4	0.15	0.3
v_{on} (V)	-5.7	-3.5	-1.5
R_{off} (Ω)	50M	10K	300K
R_{on} (Ω)	150K	1K	4K
k_{off} (m/s)	10^{-4}	5.43×10^{-10}	0.091
k_{on} (m/s)	-30	-7.34×10^{-8}	-216.2
D (nm)	10	10	3
ON time 1	(6V) 261.12ns	(4V) 713.57ms	(2V) 31.97ps
OFF time 1	(6V) 825.37μs	(4V) 953.68ms	(2V) 2.21ns
ON time 2	(7V) 97.66ns	(5V) 566.44ms	(3V) 5.03ps
OFF time 2	(7V) 540.18ns	(5V) 317.89ms	(3V) 13.88ps

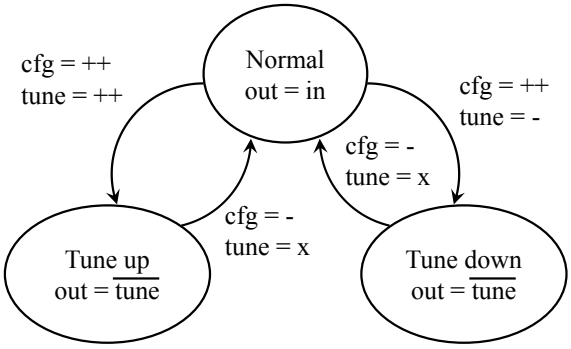


Fig. 3: State diagram for switching the operating mode of the memristor-based delay element.

III. Design of the Pulse Controlled Memristor-based Delay Element

In this section, the design of a pulse controlled memristor-based delay element is explained. We start from the top-level design to describe its operation modes and components' interfaces. The circuit design is then provided in details. Next, the memristor properties are considered to select an appropriate one. Finally, the backward tuning problem is identified and our solution is proposed.

This delay element requires two voltage supplies: V_{tune} for the memristance tuning and V_{dd} for powering the standard logic cells. In this paper we use there symbols ("$++$", "$+$", and "$-$") to represent different voltage levels, as summarized in Table II. Notice that the tuning voltage must be greater than both v_{on} and v_{off} thresholds, while the logic voltage should be lower to avoid the memristance shift in the normal mode.

TABLE II: Voltage Notations.

Symbol	Value (V)	Description
$++$	7	Memristance tuning voltage (V_{tune})
$+$	5	Logic 1 (V_{dd})
$-$	0	Logic 0 (Ground)

A. Top-level design

The delay element can operate in one of three modes that are summarized in Table III. The transition between the operating modes is controlled by cfg and $tune$ signals, as shown in the state diagram in Fig. 3.

TABLE III: Operation Modes of the Proposed Delay Element.

Mode	Signal	
	cfg	$tune$
Tune up	$++$	$++$
Tune down	$++$	$-$
Normal	$-$	either $++$ or $-$

The cfg signal selects either the tuning mode (when the delay is being configured) or the normal mode (when the input signal is passed through to the output with an additional delay). The $tune$ signal is used to control the tuning directions: either *tune up* to gain more delay or *tune down* for the opposite way. The state of $tune$ signal is ignored in the normal mode and can be either "$++$" or "$-$".

At the top level the proposed delay element consists of two control inputs cfg and $tune$, a normal input in, a delayed output out, and two voltage supply pins V_{dd} and V_{tune}, as illustrated in Fig. 4.

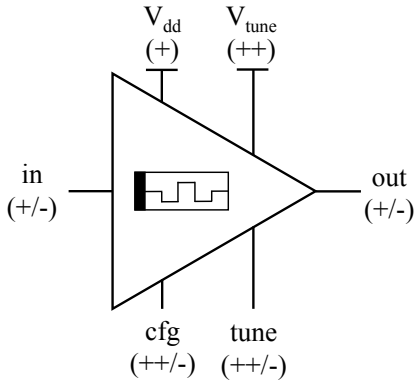


Fig. 4: Symbol for the pulse controlled memristor-based delay element.

B. Circuit schematic

The state diagram in Fig. 3 and the circuit schematic in Fig. 5 document the circuit operation. In the normal mode, the cfg is "$-$" and turns on both MP2 and MN2, which form a pass gate, to pass the normal signal from the input buffer to the memristor and then to the output buffer. The cfg also turns off both MP3 and MN3 to cut the tuning network from V_{tune} and ground whether the $tune$ is "$++$" or "$-$". In the tune up mode, the cfg switches to "$++$" and turns off the pass gate while both MP3 and MN3 are turned on. At the same time, the $tune$ is "$++$" and turns on both MP5 and MN4. This connects mem_out and mem_in to V_{tune} and ground respectively and causes the state variable to go higher. On the other hand, in tune down mode, the cfg is "$++$" which turns on both MP3 and MN3 while the $turn$ changes to "$-$" and turns on MP4 and MN5. This also connects the memristor to

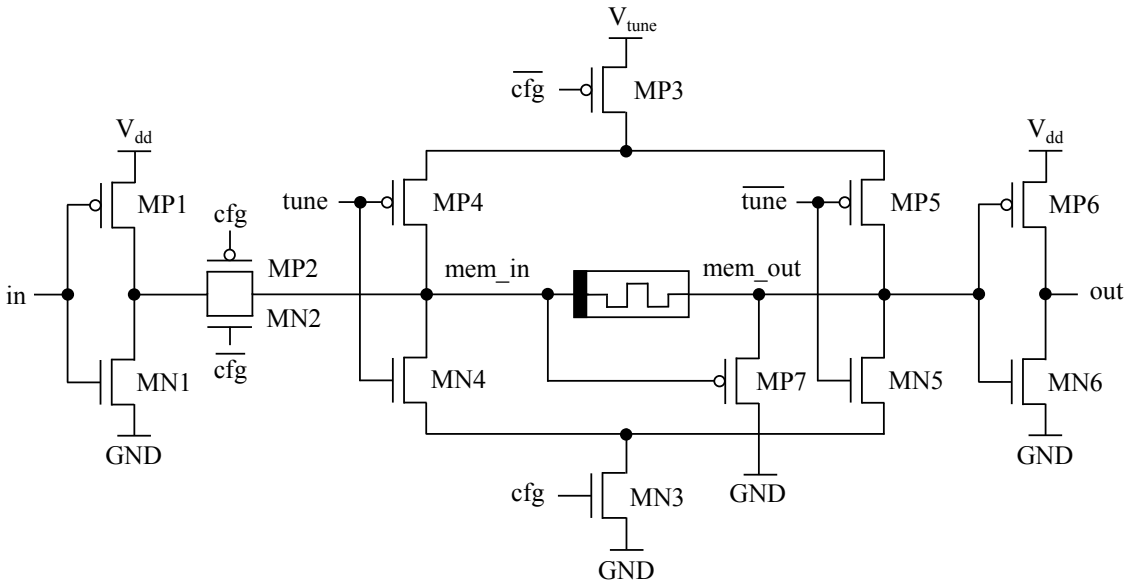


Fig. 5: Circuit schematic for the pulse controlled memristor-based delay element.

V_{tune} and ground but in the opposite direction and causes the state variable to go lower.

The transistor MP7, whose the gate and source are connected to mem_in and mem_out respectively, is used to deal with the backward tuning problem as explained in Section III-C. In addition, the pass gate is necessary to block the leakage current that flows from V_{tune} to V_{dd} via the body of MP1 which occurs in both tuning operations. Note that the memristor can be placed in both directions depending on the thresholds. The side that has the threshold above the normal signal amplitude must be attached at mem_in to avoid the memristance change. However, the memristor can be placed in any directions if both of its thresholds are greater than the mentioned amplitude.

All transistors except MP7, which will be described in Section III-C, are sized to balance the rise and fall times. For high voltage AMS CMOS 0.35μm technology, the proper W_p/W_n ratio is 1. Therefore, the widths of 40μm are selected for MP1-MP5 and MN1-MN5 while both MP6 and MN6 are sized as 20μm.

C. Memristor choosing and backward tuning problem

The memristor selection criteria comprises the thresholds, fabrication technology and total tuning time. To prevent the state variable shift by the normal amplitude, both memristor thresholds should be greater than V_{dd}. Meanwhile, they must also be within the operating voltage range of the target fabrication technology to ensure that the tuning voltage V_{tune} is applicable and the design can be practically fabricated. Both conditions are stated as (3) and (4).

$$Min(|v_{on}|, |v_{off}|) > V_{dd} \tag{3}$$

$$V_{technology} > Max(|v_{on}|, |v_{off}|) \tag{4}$$

Unfortunately, based on the VTEAM model [19], it is hard to find such memristor. For instance, the OFF thresholds of the Boundary Condition Memristor (BCM) [19] and the Memristor-Aided Logic (MAGIC) [21], as shown in Table I, are too low. Thus, the signal amplitude below them is not supported by today technologies. Although the technology can provide such voltage, it is not capable of supporting the voltage above the high ON threshold at the same time. In addition, there is another memristor which both of its threshold magnitudes are nearly equal and in the range of the regular AMS CMOS 0.35μm technology but its model parameter is not available at the moment. This limitation forces us to choose the memristor with only one satisfied threshold and face the "backward tuning problem".

The backward tuning problem happens when at least one memristor threshold is below the signal amplitude, as illustrated in Fig. 6. Assume there is a memristor with only one side that has a higher threshold than V_{dd}. Connecting this side to mem_in and the other side to mem_out seems reasonable because the normal signal cannot exceed this high threshold. However, in the normal mode, the signal at mem_out, which is the low threshold side, is delayed and causes a voltage difference $v(t)_{mem\_out} - v(t)_{mem\_in}$ between the memristor terminals. If this voltage is larger than the threshold, the state variable will shift unexpectedly. To sum up, the backward tuning problem takes place when conditions (5) and (6) are met simultaneously. Note that if the delay is not long enough, as in delay element presented in [11], then the backward tuning problem may not manifest itself.

$$V_{dd} > Min(|v_{on}|, |v_{off}|) \tag{5}$$

$$|v(t)_{mem\_out} - v(t)_{mem\_in}| > |v_{on}| \text{ or } |v_{off}| \tag{6}$$

To deal with this problem, the flushing transistor MP7 in

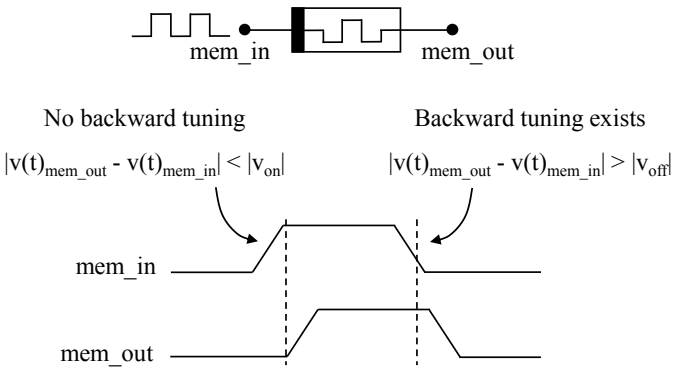


Fig. 6: Backward tuning problem.

Fig. 5 is used to flush the charges at mem_out when they are significantly greater than that at mem_in. The transistor size is selected as 100μm to keep the state variable growth at small rate. Fig. 7 shows the growth of the state variable with and without this transistor – with flushing, the growth is significantly lower. However, this solution reduces the rising delay time and causes the difference between rising and falling propagation delay as discussed in Section IV-A. Furthermore, the flushing transistor also causes a high power dissipation in tune up period because mem_in and mem_out will connect to ground and V_{tune} respectively. As a result, this transistor will conduct another current path and most of the current will be drawn through this path. The additional path affects the voltage drop at mem_out as well and, hence, slows down the tuning speed as expressed in (2). To save the power, another transistor should be connected in series with the flushing one. By using cfg as a control signal, the additional transistor will be ON in normal mode and allow usual flushing mechanism. Alternatively, it will be OFF in both tuning modes and block the current flow. This solution can reduce the tune up power consumption to the same rate as the tune down one and also decrease the tune up time because the voltage at mem_out is closer to V_{tune} than before. However, this shorter tune up time causes a great difference in tuning interval between both tuning modes and consequently requires different tuning pulse widths which increase the complexity of the delay control circuit (not in this paper). Therefore, to simplify the circuit operation by using single tuning pulse width, the aforementioned transistor is ignored.

Another factor in selecting the memristor is tuning speed which impacts the number of tuning steps. From the list of total tuning time in Table I, the MAGIC switching is the fastest and can completely turn between R_{off} and R_{on} within a single tuning step. This is useful for the systems that require only two delays. If a multiple step delay is required then the memristors with longer tuning time should be considered instead.

IV. Experiments

The experiments were conducted using high voltage AMS CMOS 0.35μm technology and VTEAM memristor model with Biolek window function [19]. The ferroelectric fitting parameter set from Table I was chosen because of its wide memristance range and ON threshold that fits with the operating voltage. Using this memristor, the V_{tune} was set above the highest threshold of 7V while V_{dd} was set as 5V to let the transistors operate correctly. Regarding a very high memristance of the selected memristor, ten identical devices were connected in parallel resulting in 15KΩ and 5MΩ as the actual minimum and maximum memristance respectively. The normal signal frequency in all experiments was set to 10MHz.

Three experiments were conducted with the following goals:

- Identify the maximum effective memristance and the maximum delay, i.e. to find the upper limit of the circuit.
- Examine the minimum tuning pulse that works well along the memristance range, and average delay per step.
- Measure the power consumption in different operating modes.

A. Maximum effective memristance and its delay

The whole memristance range is not usable because the over memristance causes internal signal distortion and results

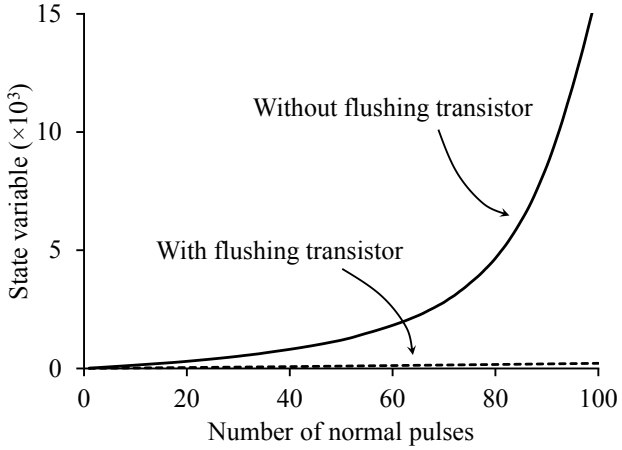


Fig. 7: The growth rate of the state variable with and without flushing transistor.

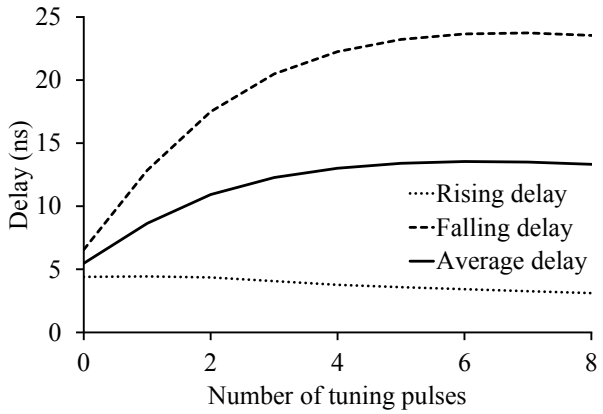
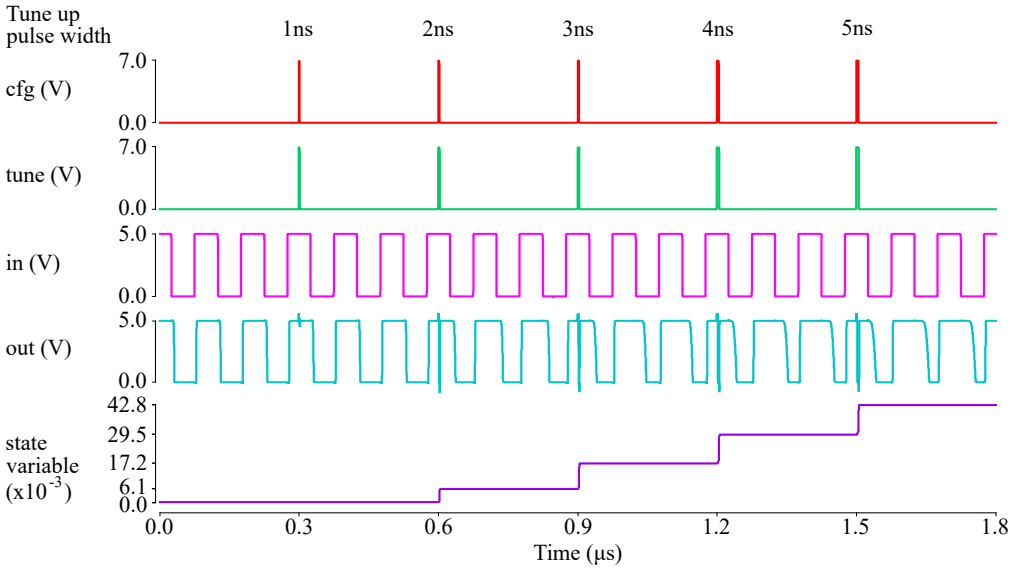
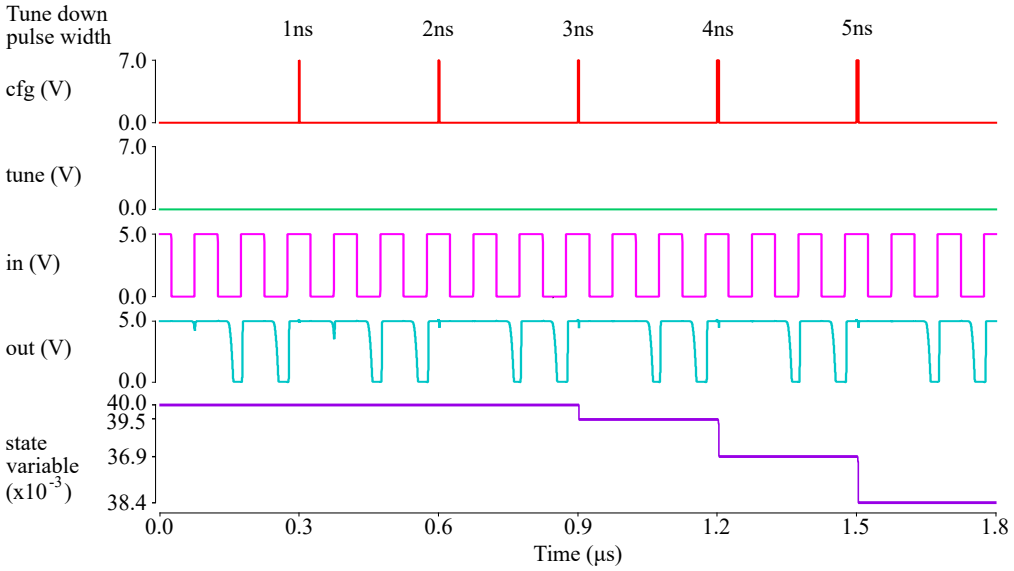


Fig. 8: The relation of tuning pulses VS delay (pulse width: 3ns).



(a) Tune up mode.



(b) Tune down mode.

Fig. 9: Simulation results for identification of the minimum tuning pulse width.

in delay saturation, where increasing of the memristance does not impact the delay anymore. The maximum memristance can be observed by applying tuning pulses (3ns pulse width) in tune up mode until the delay saturates. From the simulation results in Fig. 8, the average delay grows exponentially and saturates at the 6th pulse which indicates the maximum delay of 13.54ns and the state variable value of 40×10^{-3}. This value can be converted to the maximum effective memristance of 214KΩ using equation (1).

According to the effect of the flushing transistor, the rising delay remains low because the charges are flushed quickly. The large difference between the rise and fall times still exists even the widths of MN1 and MP6, which relate to the rise time, are decreased. In addition, the minimum delay and average delay per step are obtained as 5.48ns and 1.34ns respectively.

B. Minimum tuning pulse width and average delay step

To find the minimum tuning pulse width and the average delay step values, a simulation was run by sweeping the tuning pulse width in tune up mode from 1ns to 5ns with 1ns increment per step. The waveforms in Fig. 9a indicate the state variable started to increase at the 2ns pulse width. In tune down mode the state variable was initialized to the maximum effective memristance from Section IV-A. The simulation results in Fig. 9b reveals the minimum pulse width of 3ns instead. The pulse width variation comes from the difference in

TABLE IV: Specification Comparison.

Work	Range of memristance (Ω)	Delay (s)		Threshold (V)		Voltage (V)		Step time (s)	Normal mode power (W)		Tuning energy (J)	Transistor count	Technology model
		Min	Max	ON	OFF	Tuning	Logic		Static	Dynamic			
[14]	No memristor	2.06n	2.42n	No memristor		1.8	1.8	$\geq$ 2p	170μ - 340μ	N/A	N/A	11 + No. input vector	0.18μ
[15]	No memristor	7.1n	15.6n	No memristor		5	5	1.06n	3p	666μ	9.16p	70	0.35μ HV
[16]	No memristor	0.5n	5.5n	No memristor		0-1.2	1.8	4.2n	50μ	N/A	N/A	18	0.18μ
[17]	1K-10.5K	30n	3μ	N/A	N/A	N/A	1.2	N/A	N/A	N/A	N/A	7	N/A + Biolek
[18]	100-16.1K	809p	822p	N/A	0.5	N/A	0.9	N/A	N/A	N/A	N/A	5 + interface	40n + Modified Biolek
[11]	6K-45K	N/A	140p	0.75	-0.75	0.95	0.95	N/A	N/A	N/A	N/A	10 + 2 inverters	45n + Modified Yakopcic
This	15K-214K	5.48n	13.54n	-5.7	1.4	7	5	1.34n	14p	203μ	42p / 1.4p	13 + 2 inverters	0.35μ HV + VTEAM

memristances: the lower one allows the signal to swing faster. In order to use the same pulse width for the whole range, the 3ns pulse was assigned as the minimum tuning pulse width for all the experiments.

It is notable that the glitches in out signal in Fig. 9a were initially ignored as the solutions depend on the system implementation strategies. For instance, it can be adopted with the clocked circuit without modification as the glitches that occur between the clock edges do not affect the flip-flop [11]. Instead, replacing the last stage buffer by the tri-state one is useful for asynchronous circuit implementations. Additionally, from out signal in Fig. 9b, the first output after tune down operation was missing due to all internal charges at mem_out were wiped and could not be restored in time. A solution of this issue is subject of the future work.

C. Power consumption

The static and dynamic power consumption are measured separately: The static power of 14pW is observed as an average value from all combinations of the DC input signals (in and $tune$). The dynamic power of 203μW is measured when a pulse train is applied at in. Note that we also use this measurement method for the multiplexer-based delay element which is discussed in the next section.

The energy for the tune up and tune down operations is measured when the 3ns-width pulses are sent to both cfg and $tune$ terminals. The energy readings of 42pJ and 1.4pJ are observed as the results of the tune up and tune down respectively. The tune up energy per pulse is significantly higher due to the flushing transistor, as explained in Section III-C. Although the tune down energy per pulse is approximately 40 times lower, it may require more pulses due to the slower memristance shifting speed, thus resulting in a higher total tuning energy. Overall, this circuit is eligible for the applications that do not need to adjust the delay frequently. All simulation results are summarized in Table IV.

V. Discussion

Table IV overviews the reported results from the recent works and compares them against the proposed solution.

The current-starved inverter based design in [14] can range in 360ns with a 5-bit parallel control. This circuit consumes more power in normal mode, even though the technology is smaller, because the current mirror always connects the power source to the ground. Moreover, this solution are vulnerable to the process variation as it depends on precise sizing of the transistors.

The multiplexer-based delay element in [15] replicated in the same technology as our work consumes higher dynamic power due to the higher number of logic gates. Its comparison to our circuit is discussed at the end on the section.

The circuit in [16] provides an accurate delay control with the smallest static power dissipation. By using a comparator based design, the delay shifts linearly with lower power consumption than the current-starved inverter based design. However, it needs an analog control which makes it hardly suitable for the digital applications.

The circuit in [17] gains the widest range at 2.97μs. Nevertheless, it uses a memristor as part of a current mirror, so there is still a current path that always draws energy, the same as [14]. Although this works reports the smallest number of transistors, this does not include the transistors for the memristor control circuit.

The design in [18] yields a short delay range at 13ps due to the narrow memristance boundary. By connecting a memristor in series with the pull-down path, the delay happens only on the rising transition, so another memristor and the memristance matching are required in order to provide the same delay for the falling transitions. Furthermore, the voltage divider structure limits the maximum memristance and thus the achievable delay. This happens because an increase in

memristance induces more voltage but this voltage cannot exceed the threshold at the same time.

The circuit in [11] offers a short delay with extremely low energy per transition in normal mode. Unfortunately, the provided information are not comparable with our work in term of power. Besides, the use of a modified threshold memristor cannot guarantee the circuit to be implementable. Moreover, this threshold is lower than the supply voltage which increases the risk of the backward tuning problem when the memristance grows beyond the upper limit.

Finally, our work provides an implementable design based on empirically extracted memristor parameters that contain wide spreads of the threshold voltage and the backward tuning effect. The delay in the range between 5.48ns and 13.54ns is easy to tune by controlling either the pulse width or the pulse count on a pair of control signals. The memristor position between two inverters prevents short circuit paths and therefore reduces the power consumption in normal mode, which is our main focus. From the comparison table, the dynamic power dissipation is three time lower than that of the multiplexer-based delay element. While our design has higher static power consumption, it is still better for the duty cycle of more than 0.0000024%. For example, during 1ns of switching our circuit saves enough energy to outperform multiplexer-based design for 33ms of waiting and dissipating static power. Furthermore, even though our design is based on older technology, it spends 6-orders of magnitude less static power than the current starved inverter-based delay element.

VI. Conclusion

In this paper we conceptually proposed a design of reconfigurable delay element that is based on memristor and uses pulse control for tuning the delay. We identified the backward tuning problem and proposed a solution in order to improve the power efficiency. Based on the VTEAM model with the ferroelectric parameter set and the high voltage AMS 0.35μm technology, the experiments provided circuit characteristics including an effective delay range of 5.48ns to 13.54ns within 6 tuning steps, an average delay of 1.34ns per step and a minimum tuning pulse width of 3ns. It also showed that the energy is mostly spent in the tuning mode. Hence, this circuit is suitable for the applications that do not require frequent delay tuning. The non-volatile property allows the circuit to keep the delay value whether the power is applied or not. This saves the energy and time in startup because it does not need to initialize the whole system again. Thus, this work benefits the modern computing circuits where the energy efficiency, PVT variation tolerance, reliability and lifetime become the major issues. In the future, other memristors, such as [22] and [23] will be investigated for implementations in smaller fabrication technologies. Also better solutions for the backward tuning problem will be researched.

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