Design and Analysis of High Mobility Enhancement Mode 4H-SiC MOSFETS Using a Thin SiO_2 / Al_2O_3 Gate Stack

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***Abstract*— High performance 4H-SiC MOSFETs have been fabricated, having a peak effective mobility of 265 $cm^2/V.s$, and a peak field effect mobility of 154 $cm^2/V.s$, in 2 µm gate length MOSFETs. The gate stack was designed to minimise interface states and comprised a 0.7 nm thermally grown SiO_2 on 4H-SiC, followed by Al_2O_3 and a metal gate contact. In this way carbon remaining following SiC oxidation is significantly reduced. A density of interface traps in the range 6×10^{11} - 5×10^{10} $cm^{-2}eV^{-1}$ is also obtained. Temperature dependent electrical data reveals that the high mobility results from conduction being phonon-limited rather than Coulomb-limited. Furthermore, universal mobility in these 4H-SiC MOSFETs is shown to be up to 50% of that observed in Si devices. Expressions for electric field dependent contributions to mobility are presented. A steep sub-threshold slope of 127 mV/dec indicates low electrical defect density. A temperature coefficient of -4.6 mV/K in threshold voltage is similar to that in Si MOSFETs.**

***Index Terms*— 4H-SiC MOSFET, channel mobility, phonon limited mobility, MOS devices, power semiconductor devices, universal mobility**

I. Introduction

THE MOSFET (Metal Oxide Semiconductor Field Effect Transistor) has dominated electronics for many years. This has been made possible not least because of the remarkably good interface between the semiconductor Silicon (Si) and its native oxide, the dielectric silicon dioxide (SiO_2). The interface is abrupt and any dangling bonds resulting from Si oxidation can be readily passivated by hydrogen (H). This has made Si the electronic material of choice from logic to power electronics. Silicon Carbide (SiC) is another semiconductor whose native oxide is SiO_2. But the oxidation of SiC to form SiO_2 leaves residual carbon (C), whose effect on conduction continues to be the subject of debate. Some C may react with excess O and is removed as CO or CO_2 [1]. But the remaining C may be incorporated into the growing SiO_2, giving rise to slow oxide traps (i.e. near interface traps, NITs) or else be injected into the SiC [2,3].

Following oxidation, C defects are known to exist in a number of charge states, both in SiO_2 and in SiC, with evidence from experimental techniques such as deep level transient spectroscopy (DLTS) [4] as well as theoretical techniques such as density functional theory (DFT) [5]. C may also form complex clusters involving C, O or Si. The presence of these C related defects, close to the SiC/SiO_2 interface, is likely to lead to a high density of interface traps (D_{it}). Moreover, coulombic scattering resulting from these charged defect states is known to be a significant contributor to low mobility [6].

SiC has many properties superior to Si, such as high breakdown electric field and excellent thermal conductivity, which make it attractive for power electronics [7] and for harsh environments [8]. But a key challenge for SiC MOSFET technology has been the quest for a high channel mobility. Using a conventional thermal oxidation approach, mobilities less than 10 $cm^2/V.s$ are typically obtained [9,10]. This is about two orders of magnitude below the bulk mobility of 4H-SiC, the polytype most commonly investigated for power electronics applications [11]. Post oxidation annealing (POA) in nitric oxide (NO) [12,13] or nitrous oxide (N_2O) [14,15] is known to passivate defects, but rarely leads to mobilities above 50 $cm^2/V.s$.

An alternative approach has been to use deposited dielectrics and in particular high dielectric constant (so called high-k) materials, such as metal oxides [16,17]. In this way oxidation is eliminated and so defects arising from residual C cannot arise. In many cases, the "deposited dielectric" approach fails to give mobilities above 50 $cm^2/V.s$. This is likely to be due to a poor SiC/oxide interface quality, notwithstanding the elimination of C related defects from SiC oxidation. This problem has been mitigated either by post oxidation annealing [13] or by the insertion of an interfacial layer [18, 19, 20]. Lichtenwalner *et al* [18] demonstrated a peak field effect mobility (μ_{FE}) of 106 $cm^2/V.s$ by NO annealing to form a 1-2 nm interfacial oxide prior to Al_2O_3 deposition of thickness 25 nm. Hatayama *et al* [19] reported a study comprising interfacial oxide layers up to 3.1 nm between SiC and the deposited Al_2O_3 of about 70 nm thickness. They found high peak μ_{FE}, up to 294 $cm^2/V.s$, provided an interfacial oxide < 2 nm thick is used. Yang *et al* [20] inserted 1 nm of lanthanum silicate (La_2O_3) before SiO_2 deposition to achieve a peak μ_{FE} of 133 $cm^2/V.s$.

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Arith *et al* [21] have recently reported preliminary results of increased mobility in enhancement mode 4H-SiC MOSFETs using a thin SiO_2 / Al_2O_3 gate stack to achieve a peak field effect mobility of 125 cm^2/V.s. In this paper we present a more in-depth study of such an approach. We cover the device design and present an analysis of electrical performance. We show that an optimal interfacial oxide thickness of 0.7 nm achieves the highest channel mobilities. We further demonstrate that it is the suppression of coulomic scattering that leads to a high channel electron mobility controlled by phonon scattering. In section II we describe our experimental methods, while in section III the MOS design strategy and current-voltage (I-V) results as a function of temperature are presented. Section IV analyses mobility, demonstrating a peak effective mobility of 265 cm^2/V.s. Indeed our low thermal budget devices are shown to have a mobility behaviour as high as 50% of their silicon universal mobility counterpart, a significant advance on current SiC technology using high thermal budget. Expressions are given for the effective electric field dependence of coulombic, phonon and interface roughness contributions to mobility. The work is concluded in section V.

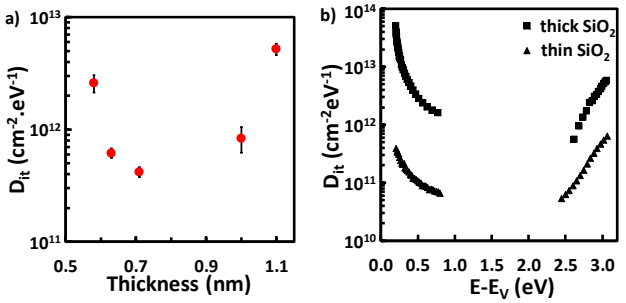

Fig. 1. Optimize the thin SiO_2 from a range of low temperature thermal budgets: a) D_{it} extracted at $E - E_v = 0.2$ eV, for each capacitor as a function of the measured oxide thickness; b) D_{it} for the MOS capacitor corresponding with the minimum D_{it} in Fig. 2a (600 ºC for 3 min). D_{it} obtained from a thick SiO_2 capacitor using conventional high temperature oxidation (1150 ºC for 180 min) is shown for comparison.

II. Experimental Methods

Both p-type and n-type MOS capacitors were fabricated on epitaxial 4H-SiC wafers, comprising a thin SiO_2 layer grown by low temperature thermal oxidation, followed immediately with around 40 nm of Al_2O_3 grown by atomic layer deposition (ALD) to achieve an effective oxide thickness (EOT) of 29 nm for the gate stack. Al_2O_3 was chosen because it is well established as a gate dielectric and available in our laboratory, with a wide bandgap (8.8 eV), good conduction band offset, remains amorphous at 1000 °C and has low levels of defect charge. The p-type wafers were supplied by Cree (3.84° off-axis, Si-face, n^+ (sub)/p^+ (10^{17} cm^{-3}, 5 µm)/p^- (5.3×10^{15} cm^{-3}, 1 µm) and the n-type by ASTRO (4.01° off-axis, Si-face, n^+ (sub)/n^+ (10^{18} cm^{-3}, 0.5 µm)/p^- (3×10^{16} cm^{-3}, 3.23 µm). The thin SiO_2 layer was grown by Rapid Thermal Processing (RTP) in a dry oxygen ambient. A range of thermal budgets with temperatures 600-800 ºC and durations between 1-3 mins were investigated. The resulting thin SiO_2 was measured by using Angle Resolved X-Ray Photoelectron Spectroscopy. The oxidation was immediately followed by growth of Al_2O_3 by ALD. Deposition was performed at 200 ºC, at a chamber pressure of 600 mTorr, with pulse/purge lengths of 0.1/4 s and 0.1/6 s for trimethylaluminum (TMA) and H_2O respectively. Alongside these "thin SiO_2" capacitors, "thick SiO_2" capacitors were fabricated on identical 4H-SiC by conventional high temperature oxidation, at 1150 ºC for 180 min in a dry O_2 ambient, resulting in a 29 nm thick SiO_2 layer. These control devices allow a direct evaluation of thin and thick SiO_2 grown by dry oxidation. Although oxidation using NO may yield a better Si/SiO_2 interface, it would introduce the role of nitrogen as an additional parameter to consider, making comparison less clear. Following analysis of the MOS capacitors, MOSFETs having both "thick SiO_2" and "thin SiO_2" gate stacks were fabricated. The process flow has been fully described elsewhere [21], resulting in a channel length (L) of 2 µm and width (W) of 100 µm. Electrical measurements were performed using an Agilent B1500A semiconductor device parameter analyzer. The density of interface traps (D_{it}) for the MOS capacitors was extracted by using the high-low method (1 MHz for high and quasi-static C-V for low frequency) [22].

III. Device Design and Electrical Performance

Our strategy for making high mobility 4H-SiC MOSFETs was to optimise the thickness of SiO_2 following low temperature oxidation during the formation of the gate stack using MOS capacitors. For each capacitor D_{it} was determined close to the energy band edges. A range of low thermal budget oxidations were investigated in order to minimize D_{it} and thereby improve MOSFET channel mobility. Oxidation temperatures between 600-800 ºC for durations of 1-3 mins resulted in thin SiO_2 layers of thickness varying from 0.58 – 1.1 nm, together with an Al_2O_3 layer to complete the gate stack. The thick deposited Al_2O_3 eliminates excessive gate leakage current by quantum mechanical tunneling through a 0.7 nm SiO_2 gate dielectric. Fig. 1a is a plot of D_{it}, extracted at $E - E_v = 0.2$ eV, for each capacitor as a function of the measured SiO_2 thickness grown during each low thermal budget oxidation. The graph shows that D_{it} passes through a minimum corresponding to a thin SiO_2 of 0.7 nm. The higher D_{it} observed as the grown oxide thickness increases may be due to increased residual C related defects and corresponding interface traps. The increase in D_{it} observed as the grown oxide thickness decreases is believed to correspond with incomplete coverage of grown oxide across the SiC giving rise to un-passivated SiC that increases interface traps. Fig. 1b shows D_{it} for the MOS capacitors corresponding with the minimum D_{it} in Fig. 1a, which occurs for a thermal budget of 600 ºC for 3 min and corresponds with 0.7 nm growth of thin SiO_2. D_{it} is plotted as a function of energy above the valence band maximum ($E-E_v$) for the entire band gap, obtained experimentally using the high-low method from p-type and n-type MOS capacitors. D_{it} obtained from thick SiO_2 capacitors using conventional high temperature oxidation at 1150 ºC for 180 mins are shown for comparison. It can be seen that D_{it} levels in the range from 6×10^{11} - 5×10^{10} $cm^{-2}eV^{-1}$ were measured using the optimum thin SiO_2 MOS capacitors. This represents a reduction in D_{it} by up to 2 orders

of magnitude compared to MOS capacitors fabricated with the thick-SiO_2 process.

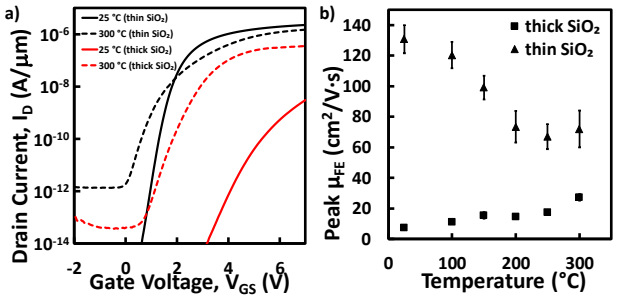

Fig. 2. (a) Drain current (I_D) versus the gate voltage (V_{GS}) with drain voltage (V_{DS}) held constant at 100 mV for MOSFETs fabricated with both the "thick-SiO_2" and the "thin-SiO_2" processes. Measurements at 25 ºC (room temperature) and at 300 ºC are shown; b) peak μ_{FE} for thin-SiO_2 MOSFETs decreases when temperature increases corresponding to phonon scattering, whereas thick-SiO_2 MOSFET mobility increases with temperature corresponding to coulombic scattering.

MOSFETs were fabricated using the gate stack comprising a thin SiO_2 interface layer of 0.7 nm, optimized to minimize D_{it}, combined with a deposited Al_2O_3 to achieve an effective oxide thickness of 29 nm. Conventional high temperature oxidation was used to produce a 29 nm thick SiO_2 gate stack for comparison. Fabricating all devices with the same effective oxide thickness (EOT) allows for a more direct comparison between device electrical properties because the gate capacitance per unit area (C_{ox}) is the same. Fig. 2a shows the drain current per unit gate width (I_D) versus the gate voltage (V_{GS}) with drain voltage (V_{DS}) held constant at 100 mV for MOSFETs fabricated with both the "thick-SiO_2" and the "thin-SiO_2" processes. Measurements at 25 ºC (room temperature) and at 300 ºC are shown. At both temperatures all devices are behaving in enhancement mode, with the off-state current I_{OFF} = 1.8 x 10^{-12}A/μm when V_{GS} = 0 V and V_{DS} = 100 mV at 300 ºC for the thin–SiO_2 SiC MOSFET. The threshold voltage (V_{th}) is taken to be V_{GS} when I_D = 10^{-10} A/μm. For MOSFETs having a thick-SiO_2 gate stack, V_{th} = 4.9 V at 25 ºC that decreases to 1.85 V at 300 ºC, while for the thin-SiO_2 gate stack, V_{th} = 1.25 V at 25 ºC that drops to 0.4 V at 300 ºC. A big improvement in the magnitude of drain current for the thin-SiO_2 MOSFETs compared with thick-SiO_2 MOSFETs is observed, for the same gate overdrive voltage (V_{GS}-V_{th}) at all temperatures. These data are consistent with Fig.2b, which shows high peak μ_{FE} in thin-SiO_2 devices up to 300 ºC.

The scattering mechanisms that dominate mobility in our 4H-SiC MOSFETs are revealed by the temperature dependence of peak μ_{FE} in Fig. 2b. Temperature dependent data plotted here (and elsewhere in the paper) represent an average of 6 devices with error bars corresponding to the standard deviation. The mobility of thin-SiO_2 devices decreases when temperature increases whereas thick-SiO_2 device mobility increases with temperature. This opposite temperature dependence suggests that different mechanisms dominate mobility in each case. Phonon scattering leads to reduced mobility with increasing temperature due to greater lattice vibration. Coulombic scattering leads to increasing mobility with increasing temperature because interaction time reduces. The temperature dependence of the semiconductor / oxide interface (roughness) scattering is weak [23]. Therefore the temperature dependence of data in Fig. 2b indicates that phonon scattering dominates mobility for the thin-SiO_2 devices, while coulombic scattering dominates mobility for the thick-SiO_2 devices. Average peak μ_{FE} of thin-SiO_2 MOSFETs decreases with temperature from 130 cm^2/V.s at room temperature to approximately 72 cm^2/V.s at 300 °C. The density of charged interface traps is believed to be the major factor associated with coulombic scattering [6]. The low value of D_{it} found in our thin-SiO_2 devices therefore corresponds with less coulombic scattering. Consequently coulombic scattering has been reduced below phonon scattering in thin-SiO_2 MOSFETs, resulting in a mobility temperature dependence with a phonon scattering signature. By contrast, the mobility for thick-SiO_2 MOSFETs increases with temperature from around 7 cm^2/V.s at 25 °C up to 28 cm^2/V.s at 300 °C. This is indicative of a higher level of coulombic scattering that dominates mobility in the control thick-SiO_2 MOSFETs.

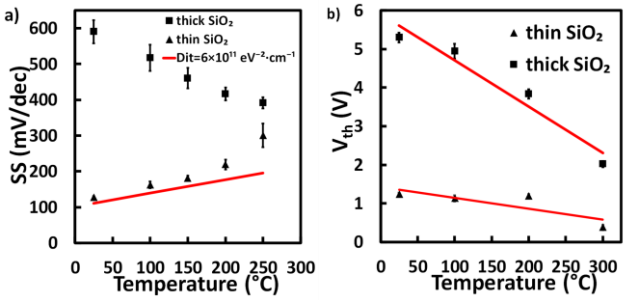

Fig. 3. Temperature dependence of MOSFET electrical parameters: a) shows the temperature dependence of MOSFET sub-threshold slope, S, showing good agreement with a plot of (1) with n derived from D_{it} b) dependence of V_{th} on temperature is much less for thin-SiO_2 MOSFETs (-4.6 mV/K) than thick-SiO_2 MOSFETs (-11.8 mV/K).

The subthreshold slope (S) is the inverse gradient of the transfer characteristic, Log I_d versus V_{GS}, and gives a measure of both electrostatic control and average interface state density [24]. Because there is an exponential dependence of I_D on V_{DS} in the subthreshold regime, S is given by:

$$S = n\frac{kT}{q}\ln(10) \qquad (1)$$

For an ideal MOSFET n=1 and S = 60 mV/dec. Values of subthreshold slope, S, were extracted from the plots of I_D versus V_{GS} in the subthreshold region where 10^{-11} > I_D > 10^{-12} A/μm. For thick-SiO_2 MOSFETs S = 590 mV/dec, while for thin-SiO_2 MOSFETs S = 127 mV/dec, indicating a large reduction in defect density in the thin-SiO_2 MOSFETs compared with the thick-SiO_2 devices. Fig. 3a shows the temperature dependence of S for our devices. It can be seen that for the thin-SiO_2 MOSFETs there is a linear increase in S with temperature, in accordance with (1). The subthreshold slope parameter, *n*, in (1) can be written as [22, 24]:

$$n = \frac{C_{ox}+C_{dep}+C_{it}}{C_{ox}} \qquad (2)$$

where C_{dep} is depletion capacitance per unit area and C_{it} is the capacitive term per unit area associated with D_{it}. The depletion capacitance C_{dep} is about an order of magnitude smaller than

either C_{ox} or C_{it}. The maximum value of D_{it} from Fig.1b is 6 x 10^{11} $cm^{-2}.eV^{-1}$. Inserting this in (2) along with other device parameters, it is found that n = 1.88. This value of n is used in (1) to plot the solid line in Fig.3a. In this way we compare S from the MOSFET transfer characteristic with S determined from D_{it}, as a function of increasing temperature. There is good agreement between the two, particularly for temperatures up to 200 °C. By comparison, the maximum value of D_{it} for the thick SiO_2 device from Fig.1b is 5 × 10^{13} $cm^{-3}.eV^{-1}$, which would give n = 67 in (2). Such a high value of n has no physical meaning for the thick-SiO_2 MOSFET data, where S is in the range of 500 mV/dec and has a negative temperature gradient. Our thick-SiO_2 device data may be better understood by including a temperature dependence in n so that differentiation of (1) becomes:

$$\frac{dS}{dT} = (n + T\frac{dn}{dT})\frac{k}{q}\ln(10) \quad (3)$$

Fig.3a shows that $\frac{dS}{dT} < 0$ for the thick-SiO_2 MOSFETs. This temperature dependence must correspond to a negative $\frac{dn}{dT}$ as all other terms in (3), on the right-hand-side, must be positive. It is speculated that this temperature dependence in n must arise from C_{it} and therefore D_{it}, which is large for thick-SiO_2 MOS gates processed with a high thermal budget (Fig. 1b). This must correspond with a high density of C related defects having a complex array of charge states in the gap that change occupancy (and therefore charge state) with increasing temperature.

Fig. 3b shows the dependence of V_{th} on temperature for both thin-SiO_2 and thick-SiO_2 MOSFETs. In both cases V_{th} decreases with increasing temperature. The decrease is commonly described by a linear temperature coefficient for Si MOSFETs [25] and there will be a similar temperature dependence for SiC devices [26]. It can be seen in Fig. 3b that the slope is significantly steeper for the thick-SiO_2 devices (-11.8 mV/K) compared with thin-SiO_2 devices (-4.6 mV/K). A decrease in V_{th} between -2mV/K and -4 mV/K occurs in n-channel Si MOSFETs depending on channel doping, corresponding to changes in the Fermi potential with temperature [27]. The larger T-dependence, particularly observed for the thick-SiO_2 MOSFETs, may arise from defects changing charge state in the channel.

IV. Mobility

High electron mobility is observed in 4H-SiC MOSFETs fabricated with the thin-SiO_2 process. Field-effect mobility μ_{FE} is commonly used as a figure of merit for SiC MOSFETs and is used here for purposes of comparison with other work reported in the SiC literature. It can be calculated from MOSFET electrical measurements by [22]:

$$\mu_{FE} = \frac{L\, g_m^i}{WC_{ox}V_{DS}} \quad (4)$$

where g_m^i is the intrinsic transconductance [28], V_{DS} is the source-drain voltage and C_{ox} is measured using a split C-V configuration. It is often plotted as a function of effective electric field, E_{eff}, in the gate oxide resulting from the gate overdrive voltage (V_{GS}-V_{th}), and calculated from [29]:

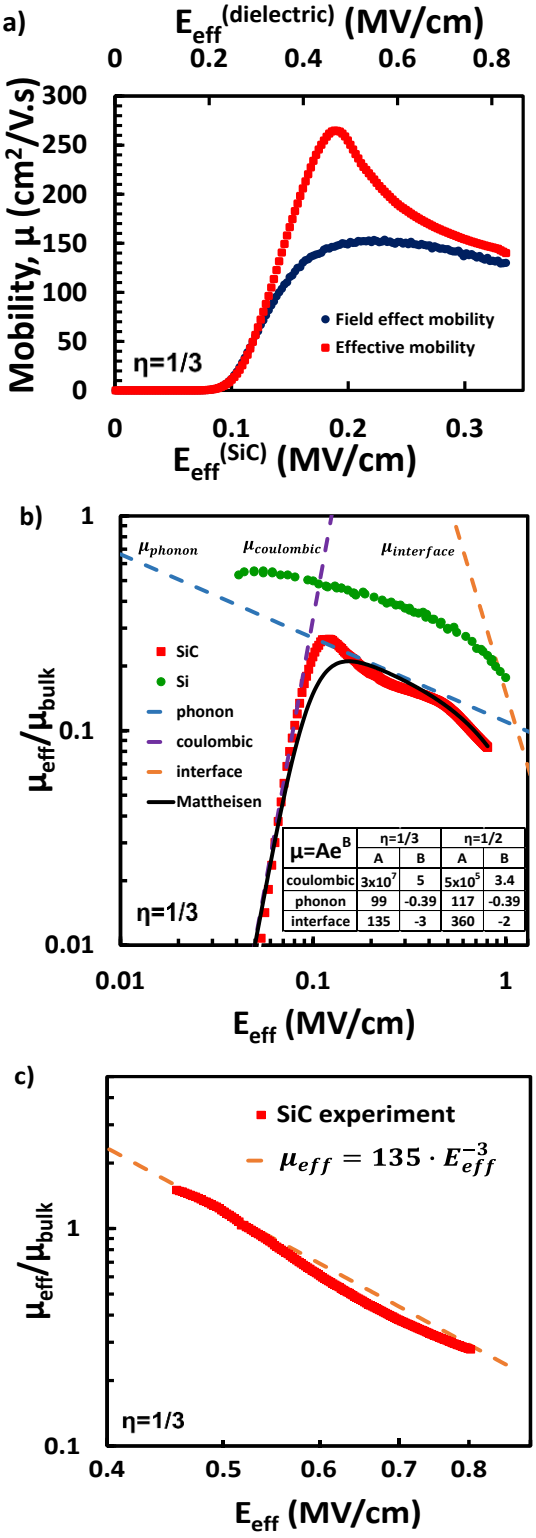

Fig. 4. Mobility as a function of increasing effective electric field E_{eff} in SiC resulting from the applied V_{GS}: a) is a comparison of μ_{FE} and μ_{eff} from the same I-V data; b) shows that normalised universal mobility (μ_{eff} /μ_{bulk} versus E_{eff}) for the 4H-SiC MOSFETs is 40% of Si MOSFETs [29] (contributions from $\mu_{coulombic}$ and μ_{phonon} are also illustrated); c) $\mu_{interface}$ plotted alongside the extracted experimental MOSFET data for interface (roughness) limited effective mobility.

$$E_{eff} = \frac{q}{\varepsilon_0 \varepsilon_{SiC}}\left(N_{depl} + \eta N_S\right) \quad (5)$$

where ε_{SiC} is the relative permittivity of SiC, N_{depl} is the depletion charge density under the gate, N_S is the inversion charge density and η is a weighting function for N_S that depends on substrate orientation. For Si MOSFETs η = ½ for electrons on the (100) face, while η = 11/32 is obtained theoretically [30]. Ohashi et al [31] have shown that η = 1/3 is a better fit to mobility data in C faced SiC MOSFETs and is expected to be the case for Si faced SiC MOSFETs too.

Fig. 4a shows a plot of μ_{FE} as a function of E_{eff} (η = 1/3) in the SiC close to the oxide interface. For ease of comparison, E_{eff} in the gate dielectric is indicated on the same graph. This is taken to be equivalent to SiO_2 and so given by E_{eff} in SiC scaled by the permittivity ratio $\frac{\varepsilon_{SiC}}{\varepsilon_{SiO2}}$. It can be seen that μ_{FE} peaks at 154 cm^2/V·s for E_{eff} = 0.23 MV/cm in SiC, which corresponds to a gate overdrive voltage (V_{GS}-V_{th}) of 3.5 V. Field effect mobility μ_{FE} remains above 130 cm^2/V·s up to a gate overdrive of 6 V, corresponding to E_{eff} = 0.35 MV/cm (η = 1/3) in the SiC and E_{eff} = 0.87 MV/cm in the gate oxide.

Effective mobility, μ_{eff}, is more commonly used as a figure of merit for Si MOSFETs [29]. It is frequently plotted as a function of E_{eff} in the semiconductor in part because this is where the electron channel is located but also because the gate dielectric may not be SiO_2 but a deposited high-k dielectric [29]. A plot of μ_{eff} versus E_{eff} is known as a "universal mobility curve" because it is independent of substrate impurity concentration or bias. Effective mobility can be calculated from MOSFET measurements by:

$$\mu_{eff} = \frac{L\, g_d^i}{W Q_n} \quad (6)$$

where g_d^i is the intrinsic channel conductance and Q_n is the mobile channel charge density, which is calculated from the gate-to-channel capacitance per unit area, C_{GC}, according to [22]:

$$Q_n = \int_{-\infty}^{V_{GS}} C_{GC}\, dV_{GS} \quad (7)$$

Capacitance measurements, using split C-V, were carried out at 10 kHz. C-V plots 10 kHz - 1 MHz show negligible frequency dispersion. Fig. 4a also includes a plot of μ_{eff} versus E_{eff} for the thin-SiO_2 in order to compare it with μ_{FE}. It can be seen in Fig. 4a that μ_{eff} peaks at 265 cm^2/V.s and remains higher than the value of μ_{FE} over the whole range of E_{eff} measured. Differences between μ_{eff} and μ_{FE} can be accounted for if the measured C_{GC} has a major contribution from trapped charge [32]. We obtain a trap charge density, Q_{it}, of $3.6 \times 10^{-8}\ C/cm^2$ by integration under the curve for D_{it} in Fig. 1b:

$$Q_{it} = q \int_{E_i}^{E_c} D_{it}\, F_{\frac{1}{2}}(E) dE = 3.6 \times 10^{-8}\ C/cm^2 \quad (8)$$

Where E_c is the conduction band minimum, E_i is the intrinsic energy and $F_{1/2}$ is the Fermi function. From (7) the total charge at peak μ_{eff} is 3.67 x 10^{-7} C/cm^2, so less than 10% of the charge contribution to C_{GC} is trapped charge. Instead the discrepancy between μ_{eff} and μ_{FE} is mainly due to the omission of electric field dependence in the calculation of μ_{FE} in (4) [22].

The mobility in 4H-SiC MOSFETs has been notoriously poor compared to Si counterparts, but the intrinsic bulk electron mobility is of a comparable magnitude, being 900 cm^2/V.s for 4H-SiC and 1450 cm^2/V.s for Si. So low mobility in 4H-SiC MOSFETs fabricated using a high thermal budget gate oxidation results from the resulting poor interface between SiC and SiO_2.The performance of our 4H-SiC MOSFETs can be compared with Si MOSFETs by plotting universal mobility curves. For a fair comparison the device mobility is normalised against the intrinsic bulk mobility of the semiconductor. Fig. 4b shows normalised universal mobility curves for 4H-SiC and Si MOSFETs in a log plot of normalised mobility as a function of E_{eff} (η = 1/3) in the semiconductor. The plot reveals that channel mobility in Si MOSFETs varies from 55% to 18% of the bulk Si mobility as E_{eff} in the Si increases to 1 MV/cm as a result of increasing V_{GS}. By comparison, the channel mobility in SiC MOSFETs varies from 27% to 7% of the bulk SiC mobility over the same range of E_{eff}. This means that the SiC MOSFETs are achieving up to 50% of the performance observed in Si MOSFETs throughout the range of E_{eff} up to 1 MV/cm, which corresponds with E_{eff} = 2.5 MV/cm in the gate oxide or an applied V_{GS} = 13 V in our thin-SiO_2 MOSFETs with an EOT of 29 nm.

Several scattering processes impact MOSFET mobility, which can be represented by Matthiesen's rule:

$$\frac{1}{\mu} = \frac{1}{\mu_{coulombic}} + \frac{1}{\mu_{phonon}} + \frac{1}{\mu_{interface}} \quad (9)$$

The first term $\mu_{coulombic}$ corresponds with coulombic scattering resulting from carrier-carrier scattering and fixed charges such as interface traps or remote scattering from charged defects in the SiO_2 or SiC. The second term μ_{phonon} corresponds with phonon scattering and is material dependent. The final term $\mu_{interface}$ corresponds with (roughness) scattering at the semiconductor/oxide interface in MOSFETs, which is known to dominate mobility in Si MOSFETs for high gate voltage, V_{GS}, while coulombic scattering dominates at low V_{GS} but gives way to phonon scattering for a wide intermediate range of V_{GS} or E_{eff}. [29].

From the experimental universal mobility data shown in Fig. 4b the following expressions for coulombic-limited effective mobility ($\mu_{coulombic}$), and phonon-limited effective mobility (μ_{phonon}) as a function of E_{eff} (η = 1/3) can be determined:

$$\mu_{coulombic} = 3 \times 10^7 \cdot E_{eff}^5 \quad (10a)$$

$$\mu_{phonon} = 99 \cdot E_{eff}^{-0.39} \quad (10b)$$

These relationships are plotted as dashed lines in Fig. 4b. Because some uncertainty remains in the value of η, expressions for effective mobility as a function of E_{eff} (η = ½) are also derived:

$$\mu_{coulombic} = 5 \times 10^5 \cdot E_{eff}^{3.4} \quad (11a)$$

$$\mu_{phonon} = 117 \cdot E_{eff}^{-0.39} \quad (11b)$$

Comparing with Noguchi *et al* [33], we note our phonon-limited mobility follows the same E_{eff} dependence, but is 75% higher. Interface (roughness) limited effective mobility ($\mu_{\text{interface}}$) is not dominant up to E_{eff} = 0.7 MV/cm, but can be determined using (9) and subtracting coulombic and phonon contributions. In this way expressions for interface limited effective mobility as a function of E_{eff} can be determined:

$$\mu_{interface} = 135 \cdot E_{eff}^{-3} \quad (\eta = 1/3) \qquad (12a)$$

$$\mu_{interface} = 360 \cdot E_{eff}^{-2} \quad (\eta = 1/2) \qquad (12b)$$

Equation (12a) is plotted alongside the extracted experimental MOSFET data for interface (roughness) limited effective mobility as a function of E_{eff} in Fig. 4c. In Fig.4b we include a plot of mobility, normalized against bulk mobility, as a function of E_{eff}, obtained using Matthiesen's rule (9) to combine contributions from coulombic (10a), phonon (10b) and interface roughness (12a) scattering. We believe that this is the first direct determination of the three key contributions to high mobility enhancement mode 4H-SiC MOSFETs.

V. Conclusions

High performance enhancement mode 4H-SiC MOSFETs were fabricated having a gate stack comprising 0.7 nm of SiO_2 and Al_2O_3 with an effective oxide thickness of 29 nm and channel length of 2 μm. The strategy of optimising the thickness of the SiO_2 layer using MOS capacitors to minimise D_{it} led to the choice of a low temperature oxidation of 600 °C for 3 mins. A peak effective mobility of 265 $cm^2/V.s$ was measured and device performance was shown to be up to 50% of that observed in Si MOSFETs, when compared by normalised universal mobility versus effective electric field. A peak field effect mobility of 154 $cm^2/V.s$ was determined, which remained above 130 $cm^2/V.s$ up to a gate overdrive of 6 V, corresponding to E_{eff} = 0.49 MV/cm in the SiC and E_{eff} = 1.2 MV/cm in the gate oxide. The temperature dependence of field effect mobility revealed that coulombic scattering has been sufficiently reduced to make phonon scattering the dominant mechanism controlling carrier transport. Expressions for coulombic, phonon and interface (roughness) contributions to mobility as a function of effective electric field have been determined. Temperature dependent measurements also revealed a good correspondence between the MOSFET steep subthreshold slope of 127 mV/dec and a subthreshold slope parameter, *n*, of 1.88 as determined by D_{it} values obtained from MOS capacitors. A temperature coefficient of -4.6 mV/K in V_{th} is close to that obtained in Si MOSFETs. We therefore conclude that the use of a thin (0.7 nm) SiO_2 layer in the gate stack to control defects related to C that remains after oxidation is a promising route for the fabrication of high performance SiC MOSFETs

References

[1] S. Wang, M. Di Ventra, S. G. Kim, and S. T. Pantelides S. Wang, M. Di Ventra, S. G. Kim, and S. T. Pantelides "Atomic-Scale Dynamics of the Formation and Dissolution of Carbon Clusters in SiO_2" *Physical Review Letters*, vol. 86, pp. 5946-5949, 2001

[2] T. Zheleva, A. Lelis, G. Duscher, F. Liu, I. Levin, and M. Das "Transition layers at the SiO_2 /SiC interface" *Applied Physics Letters.* vol. 93, p. 022108, 2008

[3] V. V. Afanas'ev, A. Stesmans, F. Ciobanu, G. Pensl, K. Y. Cheong, and S. Dimitrijev "Mechanisms responsible for improvement of 4 H–SiC/SiO_2 interface properties by nitridation" *Applied Physics Letters*, vol. 82, pp. 568-570, 2003; doi: 10.1063/1.1532103

[4] T. Hiyoshi and T. Kimoto "Elimination of the Major Deep Levels in n- and p-Type 4H-SiC by Two-Step Thermal Treatment" *Applied Physics Express*, vol. 2, p. 091101, 2009

[5] F. Devynck, A. Alkauskas, P. Broqvist, and A. Pasquarello "Charge transition levels of carbon-, oxygen-, and hydrogen-related defects at the SiC/SiO_2 interface through hybrid functionals" *Physical Review B*, vol. 84, p. 235320, 2011

[6] T. Kimoto and J. A. Cooper. Fundamentals of silicon carbide technology: growth, characterization, devices, and applications (1st ed.), Section 6.3.5, 2014, J Wiley-IEEE ISBN 1118313526, 9781118313527.

[7] L. Cheng, J. W. Palmour, A. K. Agarwal, S. T. Allen, E. V. Brunt, G. Wang, V. Pala, W. Sung, A. Q. Huang, M. O'Loughlin, A. Burk, D. Grider, and C. Scozzie, "Strategic overview of high-voltage SiC power device development aiming at global energy savings," *Mater. Sci. Forum*, vol. 778-780, pp. 1089-1095, 2014. DOI: 10.4028/www.scientific.net/MSF.778-780.1089

[8] Y. Nanen, M. Aketa, Y. Nakano, H. Asahara and T. Nakamura, "Electrical characterization of 1.2 kV-class SiC MOSFET at high temperature up to 380°C," *Mater. Sci. Forum*, vol. 858, pp. 885-888, 2016. DOI: 10.4028/www.scientific.net/MSF.858.885

[9] L. Chao-Yang, J. A. Cooper, T. Tsuji, C. Gilyong, J. R. Williams, K. McDonald and L. C. Feldman., "Effect of process variations and ambient temperature on electron mobility at the SiO2/4H-SiC interface," *IEEE Trans. Electron Devices*, vol. 50, no. 7, pp. 1582-1588, 2003. DOI: 10.1109/TED.2003.814974

[10] G. Y. Chung, C. C. Tin, J. R. Williams, K. McDonald, R. K. Chanana, R. A. Weller, S. T. Pantelides, L. C. Feldman, O. W. Holland, M. K. Das and J. W. Palmour, "Improved inversion channel mobility for 4H-SiC MOSFETs following high temperature anneals in nitric oxide," *IEEE Electron Device Lett.*, vol. 22, no. 4, pp. 176-178, 2001. DOI: 10.1109/55.915604

[11] S. Ryu, C. Capell, E. Van Brunt, C. Jonas, M. O'Loughlin, J. Clayton, K. Lam, V. Pala, B. Hull, Y. Lemma, D. Lichtenwalner, Q. J. Zhang, J. Richmond, P. Butler, D. Grider, J. Casady, S. Allen, J. Palmour, M. Hinojosa, C. W. Tipton and C. Scozzie "Ultra high voltage MOS controlled 4H-SiC power switching devices" *Semiconductor Sci. and Technol.*, Vol 30, p. 084001, 2015

[12] P. Jamet, S. Dimitrijev and P. Tanner "Effects of nitridation in gate oxides grown on 4H-SiC", *Journal of Applied Physics*, vol. 90, pp. 5058-5063, 2001

[13] J. Rozen, A. Ahyi, X. Zhu, J. Williams, and L. Feldman "Scaling Between Channel Mobility and Interface State Density in SiC MOSFETs" *IEEE Trans. Electron Devices*, vol. 58, pp. 3808-3811, 2011.

[14] L. A. Lipkin, M. K. Das, and J. W. Palmour, "N_2O Processing Improves the 4H-SiC:SiO_2 Interface," *Materials Science Forum*, vol. 389-393, pp. 985-988, 2002.

[15] K. Fujihira, Y. Tarui, M. Imaizumi, K.-i. Ohtsuka, T. Takami, T. Shiramizu, et al., "Characteristics of 4H–SiC MOS interface annealed in N_2O", *Solid-State Electronics*, vol. 49, pp. 896-901, 2005.

[16] R. Mahapatra, A. Chakraborty, A. Horsfall, S. Chattopadhyay, N. Wright, K. Coleman, "Effects of interface engineering for HfO_2 gate dielectric stack on 4H-SiC", *Journal of Applied Physics*, vol. 102, p. 024105, 2007

[17] C. Tanner and Y-C. Perng "Electrical performance of Al_2O_3 gate dielectric films deposited by atomic layer deposition on 4H-SiC" *Applied Physics Letters*, vol. 91, p. 203510 2007

[18] D. J. Lichtenwalner, V. Misra, S. Dhar, S.-H. Ryu, and A. Agarwal, "High-mobility enhancement-mode 4H-SiC lateral field-effect transistors utilizing atomic layer deposited Al_2O_3 gate dielectric," *Applied Physics Letters*, vol. 95, p. 152113, 2009.

[19] T. Hatayama, S. Hino, N. Miura, T. Oomori, and E. Tokumitsu, "Remarkable increase in the channel mobility of SiC-MOSFETs by controlling the interfacial SiO_2 layer between Al_2O_3 and SiC," *IEEE Trans. Electron Devices*, vol. 55, pp. 2041-2045, 2008.

[20] X. Yang, B. Lee, and V. Misra, "High mobility 4H-SiC lateral MOSFETs using lanthanum silicate and atomic layer deposited SiO_2," *IEEE Electron Device Letters*, vol. 36, pp. 312-314, 2015.

[21] F. Arith, J. Urresti, K. Vasilevskiy, S. Olsen, N. Wright, A. O'Neill "Increased Mobility in Enhancement Mode 4H-SiC MOSFET Using a

Thin SiO_2 / Al_2O_3 Gate Stack" *IEEE Electron Device Letters*, vol. 39, pp. 564-567, 2018

[22] D. K. Schroder, Semiconductor Material and Device Characterization, 3rd edition, John Wiley & Sons, 2006.

[23] S. K. Powell, N Goldsman, J M. McGarrity, and J Bernstein "Physics-based numerical modeling and characterization of 6H-silicon-carbide metal–oxide–semiconductor field-effect transistors" *Journal of Applied Physics*, vol. 92, p. 4053 2002

[24] S. M. Sze, Physics of Semiconductor Devices, 2nd Edition, John Wiley & Sons, 1981.

[25] N Weste and K Eshraghian, Principles of CMOS VLSI Design : a systems perspective, Second Edition, pp.48, 1993, ISBN 0-201-53376-6

[26] Y Goldberg, M Levinshtein, S Rumyantsev, in Properties of Advanced Semiconductor Materials GaN, AlN, InN, BN, SiC, SiGe, Ed M Levinshtein, S Rumyantsev, M Shur, pp93-148, John Wiley & Sons, 2001

[27] F Klaassen, W Hes "On the Temperature Coefficient of the MOSFET Threshold Voltage" Sol. State. Electron. Vol.29 pp787-789, 1986

[28] S. Y. Chou and D. A. Antoniadis, "Relationship between measured and intrinsic transconductances of FET's," *IEEE Trans. Electron Devices*, vol. 34, pp. 448-450, 1987. DOI: 10.1109/T-ED.1987.22942

[29] S. Takagi, A. Toriumi, M. Iwase, and H. Tango, "On the universality of inversion layer mobility in Si MOSFET's: Part I-effects of substrate impurity concentration," *IEEE Trans. Electron Devices*, vol. 41, pp. 2357-2362, 1994.

[30] S. Takagi, A. Toriumi, M. Iwase, and H. Tango, "On the universality of inversion layer mobility in Si MOSFET's: Part II-effects of surface orientation," *IEEE Trans. Electron Devices*, vol. 41, pp. 2363-2368, 1994

[31] T. Ohashi , Y. Nakabayashi, and R. Iijima "Investigation of the Universal Mobility of SiC MOSFETs Using Wet Oxide Insulators on Carbon Face With Low Interface State Density" *IEEE Trans. Electron Devices*, vol. 65, pp. 2707-2713, 2018

[32] T. Hatakeyama, Y Kiuchi, M Sometani, S Harada, D Okamoto, H Yano, Y Yonezawa, and H Okumura "Characterization of traps at nitrided SiO_2/SiC interfaces near the conduction band edge by using Hall effect measurements Applied Physics Express Vol.10 p. 046601, 2017

[33] M. Noguchi, T. Iwamatsu, H. Amishiro, H. Watanabe, K. Kita and S. Yamakawa "Determination of intrinsic phonon-limited mobility and carrier transport property extraction of 4H-SiC MOSFETs" *2017 International Electron Devices Meeting, Tech. Dig*., pp. 219-222, 2017