Abstract—Power electronic inverters are commonly used for the interfacing of distributed generation systems to the electrical power network. These electronic inverters operate in a current controlled mode to inject unity power factor sinusoidal current into the network. To prevent possible dc current injection, a mains frequency isolation transformer is often employed at the inverter output. This isolation transformer is a costly component. An alternative approach is to use current sensing and control techniques to eliminate the dc current component. One method is to use a current controller to force the output dc current to zero. Current controllers are prone to errors associated with nonlinearity and offsets in the current transducers. This paper considers a novel auto-calibrating dc link current sensing technique that eliminates the errors associated with the current transducer, and helps avoid dc current injection into the grid when using a transformerless grid connect inverter system.

Index Terms—Current controllers, power electronic inverters.

I. INTRODUCTION

ANY DISTRIBUTED generation systems, such as photovoltaic arrays, use a current controlled dc to ac inverter to inject unity power factor sinusoidal current into the grid (see Fig. 1). In general, electricity supply companies do not allow grid connection of such inverter systems unless they provide adequate means of eliminating the possibility of unwanted dc current being injected into the grid [1], [2]. This is due to concerns over substation transformer saturation [3], [4]. dc current in the network has also been linked to increased corrosion of network cabling [5]. Typically, inverter systems which have semiconductor circuits directly connected to the mains cannot be designed in such a way that guarantees unwanted dc current components will not flow into the network. Such dc components can be attributed to several factors including asymmetry in the switching of the semiconductor devices. This is caused by imbalance in the turn-on and turn-off times of the semiconductor switches, pulse width imbalance in the pulsewidth modulation (PWM) process, or possible mismatch in the alignment of the gate drive signals. Current controller errors also create unwanted dc components in the inverter output current, a major cause being the error in the actual current measurement. A mains frequency isolation transformer is therefore typically employed at the inverter output to eliminate the possibility of unwanted dc currents being injected into the grid. This isolation transformer is large, heavy, and forms a substantial cost in a grid connected system [6]. Furthermore, it contributes significantly to the inverter system losses [7]. By removing the need for this isolation transformer the market for grid connected inverter systems would be strengthened, leading to more widespread application.

One possibility is to replace the transformer with a dc blocking capacitor in the inverter output. However, this capacitor would need to have a low reactance at 50 Hz mains frequency. Therefore a large and expensive capacitor is required. An alternative approach is to use an inverter topology that is naturally capable of preventing dc current components arising at the inverter output. Very few inverter topologies exist which possess this property, although the half-bridge [8] inverter is one example. Regardless of the switching state of the inverter, one capacitor is always present in the current path, hence blocking any dc current components. Unfortunately, twice the dc link voltage of a typical H-bridge inverter is required to achieve the same rated output. The H-bridge requires a 380 V dc link to synthesize 230 Vac at the inverter output, hence a 760 V dc link would be needed by the half bridge to synthesize the same output voltage level. This impacts on the semiconductor devices used in the inverter; 1200 V IGBTs would be needed, as opposed to 600 V IGBT devices in the H-Bridge. Compared to 600 V IGBTs, higher voltage devices cannot be switched as fast, have greater switching losses and are undesirable on cost grounds. A further approach is to use current sensing and control techniques to eliminate the dc current component. One method would be to use a current controller to force the output dc current to zero. However, the main problem with this approach is that it depends upon an accurate current sensor. A number of different types of current sensor are available in power electronic applications [9], including Hall Effect current transducers, current transformers and resistive shunts. Resistive shunts are cost effective, but it is often difficult to achieve high common mode rejection with resistive shunt amplifiers. They also offer no natural isolation between the power circuit and measurement equipment. Hall Effect current sensors are widely used due to their good performance, relatively low cost and galvanically isolated principle of operation. Unfortunately these devices are prone to linearity
errors and offset drift [10], [11]. In current control applications, offset drift affects the controller accuracy at dc and nonlinearity may result in harmonic distortion which itself may produce a dc component in the system output. It is impossible to limit, with any level of certainty, the dc component in the inverter output with better accuracy than that of the current measurement device. This makes it very difficult to meet present electricity supply regulations concerning dc current injection [1], [2] using conventional current sensing and control methods. This paper therefore considers an alternative current sensing technique to help eliminate dc current components in the inverter output current. The proposed technique auto-calibrates the current sensor to compensate for any dc offsets in the current sensor. The scheme also minimizes the effect of dc components caused by current sensor nonlinearity by ensuring a symmetrical nonlinearity in the current sensor measurement. This results in a fully compensated, dc accurate, current sensor from which it is possible to accurately limit the dc component in the inverter output via current sensing and control techniques.

II. DESCRIPTION OF DC LINK CURRENT SENSING TECHNIQUE

The proposed current sensing scheme considers current control of a single-phase inverter using dc link current sensing techniques. dc link current sensing itself is not a new concept. For a long time it has been used in many applications to detect inverter shoot-through and other over-current conditions. More recently however, knowledge of the dc link current has been put to further use. In 1986, Evans and Hill-Cottingham [12] published work detailing the dc link current behaviour of a general poly-phase inverter. By determining the dc link current wave shape, it was shown that the ripple current rating of the dc link filter capacitor could be specified with greater precision. Boys [13] took the concept a step further, by using dc link current analysis to derive signals for induction motor control. By sampling preferential portions of the dc link current, the current magnitudes of the inverter output current could be determined. The technique was shown to be accurate at high-power factors, but tended to underestimate the motor current at low-power factors. Furthermore, the signals derived from the dc link current provided no phase information about the output current. Green and Williams [14] went on to describe techniques for faithful reconstruction of the motor line currents at the output of a three-phase inverter from a single dc link current sensor. The reconstruction of the line currents included both current magnitude and phase information. Through identification of the inverter switching state, it was shown that the three line currents in the inverter output could be determined via the condition of the dc link current. A resistive shunt with a high slew-rate amplifier was used as the transducer in the dc link. A digital decoding circuit determined the state of the inverter, and was used to control a set of analogue switches in an analogue circuit. By correct control of these switches, reconstruction of the three inverter line currents was possible. In 1996, Atkinson [15] described a new technique of controlling a three-phase motor via a single dc link current sensor. From dc link measurements alone, this approach determined the rectangular components of the single current vector representation of the three-phase currents. Current control was carried out through comparison of these rectangular components with reference values. A current vector error was generated, which determined the next switching pattern to be applied to the inverter.

This paper builds upon much of this work to develop a novel dc link current sensing technique. This technique involves using a dc link current sensor which can be auto-calibrated at regular intervals while still being used for the inverter output current control. For this application, the topology of interest is the H-bridge inverter (Fig. 2). If the H-bridge is switched using a unipolar switching scheme [8] then there are four main bridge switching states that arise. These are summarized in Table I. During the first two switching states, from here on called current conducting states, a voltage is applied across the output of the inverter and current flows via the dc link to the load, in this case the supply network. During these intervals it is possible to measure the output current via the dc link sensor. Depending upon the switching state of the H-bridge, the dc link current will either be equal to, or inversely equal to, the output current. The third and fourth switching states are often referred to as free wheeling states. When the inverter is in one of these states, the inductor current simply freewheels around a loop in the H-bridge. During these periods the actual dc link current collapses to zero. If the dc link current sensor output is monitored during the freewheeling periods then, due to the described offset errors in the current sensor, a zero current measurement is unlikely to be made. However, since the actual current in the dc link is known to be zero, these periods can be used to calibrate the current sensor and remove any offset present. The inverter current controller can then accurately control the dc current component in spite of drift errors in the sensor.

A. Determining the Switching State of the H-Bridge

It is necessary to know which switching states the H-Bridge is in at the time of taking a current measurement. This can be determined by studying the effect of the PWM signals on the dc link current. Fig. 3 shows a simplified switching diagram for a unipolar-switched H-Bridge inverter. In practice, the triangular switching waveform will be of a much higher frequency than the sinusoidal waveform. Also shown are the switching states
TABLE I
KEY SWITCHING STATES IN AN UNIPOLAR SWITCHED H-BRIDGE INVERTER

<table>
<thead>
<tr>
<th>STATE</th>
<th>INVERTER LEG 1</th>
<th>INVERTER LEG 2</th>
<th>DC LINK CURRENT</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.</td>
<td>T1 ON, T4 OFF</td>
<td>T2 ON, T3 OFF</td>
<td>I_{out}</td>
</tr>
<tr>
<td>2.</td>
<td>T1 OFF, T4 ON</td>
<td>T2 OFF, T3 ON</td>
<td>-I_{out}</td>
</tr>
<tr>
<td>3.</td>
<td>T1 ON, T4 OFF</td>
<td>T2 OFF, T3 ON</td>
<td>0</td>
</tr>
<tr>
<td>4.</td>
<td>T1 OFF, T4 ON</td>
<td>T2 ON, T3 OFF</td>
<td>0</td>
</tr>
</tbody>
</table>

of the four semiconductor devices. The diagram demonstrates that, provided the PWM is not over-modulated, then taking a current measurement at the peak of the modulating triangular wave ensures the H-Bridge will be in either STATE 3 or STATE 4. Both of these are freewheeling states. Which of the two states the inverter is in is not important since the freewheeling state is only required for auto-calibration purposes and this can be achieved in either case.

At the point where the modulating triangular waveform crosses zero, the H-Bridge will be in either STATE 1 or STATE 2. Both of these are current conducting states. Unlike with freewheeling states, it is important to know precisely which state the H-Bridge is in, since it determines the polarity of the inverter output current. This can be resolved by monitoring the sinusoidal PWM demand signal. Fig 3 shows that when the PWM demand is positive, the inverter must be in STATE 1, hence the dc link current is the same polarity as the inverter output current. When the PWM is negative, however, the inverter must be in STATE 2. In this case, the dc link current is the opposite polarity of the H-Bridge output current. Therefore, for output current control purposes, the dc link current measurement must be inverted in this instance. In most practical implementations, the inverter current control is carried out in software and the PWM demand is readily available. Therefore, the inverter output current can be reconstructed in software, relieving the need for additional waveform reconstruction hardware [14]. The only hardware required is a simple timing circuit, to ensure the ADC acquires a current measurement during a freewheeling period. After conversion, the data is held in a register until the processor requires it. The bridge switching state can also be deduced directly from the inverter itself, either by monitoring the gate drive signals or the state of the semiconductor devices themselves. This alleviates the need for a timing circuit. However, unlike software monitoring of the PWM demand, significant additional hardware is required to determine the switching state of the inverter.

In summary, the inverter output current reconstruction process is described by the flow chart shown in Fig. 4. Arranging for the current measurement to coincide with the peak of the PWM triangular carrier waveform ensures a freewheeling measurement, and hence an opportunity to calibrate the current sensor when the dc link current is zero. Which freewheeling state the H-Bridge is in is unimportant and does not need to be determined. Arranging for the current measurement to coincide with where the PWM triangular carrier waveform crosses zero, ensures a current conducting measurement. The current measurement can then be calibrated by subtracting the freewheeling loop measurement from the conducting loop measurement. Assessing the polarity of the PWM modulating waveform (the PWM demand) defines which current conducting state the inverter is in, and hence the polarity of the inverter output current. The inverter output current can then faithfully be reconstructed from the calibrated dc link current measurements with no dc offset error. This calibrated measurement is then applied as a current measurement signal to a conventional PI current controller (Fig. 5). From this, the PWM demand to be applied to the inverter is determined.

III. EXPERIMENTAL ARRANGEMENT

An experimental, grid connected, dc link current sensing H-bridge inverter system has been designed and constructed...
to evaluate the scheme described (Fig. 6). For evaluation purposes, the inverter, shown in Fig. 7, may be controlled by either conventional output current sensor, or via dc link current sensor measurements.

A. Inverter Design Precautions

A number of design precautions have been incorporated to maximize the performance of the inverter. In particular, a low inductance design is required [13], [16]. A commercially available H-Bridge module has been used to ensure minimum connection lengths between semiconductor devices. Careful attention has also been paid to the layout of the printed circuit board around the dc link region. A laminar dc link has also been implemented, whereby the positive rail of the dc link lies directly above the negative rail. Ideally, the shape and size of both dc link rails will be the same to minimize stray inductance. Unfortunately, including a current sensor in one of the dc link rails creates a disturbance to the preferred layout. This is an unavoidable consequence of carrying out any dc link current measurement scheme. Therefore, careful design of the dc link is crucial to minimize the impact of including the dc link current sensor. The current sensor output is interfaced to the current control hardware via an analogue to digital converter (ADC) board. This sits above the inverter module. To minimize noise and interference corrupting the signal, the distance between the sensor output and the ADC device is as short as possible. Once the measurement is in digital format, the problems of noise are virtually eliminated. When required, the current controller reads the acquired measurement.

B. External Measurement of DC Component

The dc current component in the inverter output is determined by a shunt resistor external measurement. This current measurement is purely for evaluation purposes, and performs no part of the proposed control scheme. Hence, it is worth noting that, in practice, this measurement is not required. The shunt is mounted on a large, fan assisted, heatsink to minimize heating effects. The voltage output of the shunt is passed through a sub 1 Hz cut-off frequency, low pass filter which provides significant rejection of the 50 Hz sinusoidal fundamental. The output of this filter is then connected to a handheld, battery operated, digital multimeter (DMM). The dc voltage measured by the DMM is then scaled by the shunt resistance value to determine the dc
current component. A battery-operated meter is preferred since it provides high common mode rejection.

C. Introduction of Artificial Current Sensor DC Offset

To test the effects of current sensor drift, a deliberate external dc offset is introduced by wrapping additional turns of cable around each current sensor (Fig. 8). This cable is connected to a dc power supply via a potentiometer such that the imposed dc offset current is controllable. Both Hall Effect current sensors detect this dc current, and as a result, both current measurements contain an undesirable dc offset.

IV. EXPERIMENTAL RESULTS

A 2.3 kW grid connected system has been established, which operates from a 380 V dc link, at 20 kHz PWM switching rate with 10 Arms current demand and feeding into a 230 V ac supply network voltage. For testing purposes, the inverter uses either the dc link or the conventional output current sensor. The PI current control loop is set to inject unity power factor sinusoidal current into the supply.

A. DC Link Current Behaviour

Fig. 9 shows a comparison between the behaviour of the inverter output current and the dc link current. As the diagram shows, the dc link current is made up of a series of current pulses. The characteristic of each pulse is determined by the PWM switching rate and the PWM demand. The greater the PWM demand, the wider the pulse (Fig. 10).

B. DC Link Switching Characteristics

Fig. 11(a) shows a close up of the negative falling edge of a single pulse of the dc link current waveform. This represents the H-Bridge transition from a conducting loop to a freewheel loop. The trace clearly shows it is not an ideal transition between H-Bridge states. There is a finite time before the dc link current fully collapses to zero. The initial collapse in current is very rapid, but a slower tail off period follows this. This tail off is due to the tail-current characteristic [17] of the IGBT devices in the H-Bridge inverter. The time it takes for the current to collapse to zero has implications on the interval in which it is possible to take accurate freewheel loop measurements. Taking a freewheel loop measurement before the end of the tail current period will lead to inaccuracies. The problems associated with tail-current can be avoided through the use of MOSFET devices rather than IGBTs. Unfortunately, MOSFETs are not best suited to high voltage applications. The on-state resistance of a MOSFET increases with the voltage rating of the device.
This has a negative effect on the performance of the application within which the device is used. To enable a grid-connected inverter to synthesize the 240 V network supply at the inverter output, without the use of a stepup transformer, the inverter must operate from a dc link of around 380–400 V. For this type of application therefore, a minimum 500-V rated device would be required. In general, at voltages above 250 V the on-state resistance of a MOSFET becomes sufficiently large that its performance is not competitive to that of an IGBT.

Fig. 11(b) shows a close up of the positive rising edge of a single pulse of the dc link current waveform. This positive rising edge represents the H-Bridge transition from a freewheel state to a conducting state. Once again, the switching waveform is less than ideal. After the initial switch on characteristic, a ringing is observed in the dc link current waveform. This behaviour is due to the reverse recovery of the opposing diode causing an initial current overshoot and parasitic inductance in the inverter design causing oscillations in the current waveform at switching intervals. Even when taking great care to produce a low stray inductance layout in the power inverter PCB, a certain amount of oscillation is still noticeable. This highlights the critical importance of the circuit layout. The introduction of the dc link current sensor will be partly responsible for this phenomenon since it compromises the ideal layout of the dc link PCB design.

The behaviour of the dc link during the rising edge of a current pulse has implications on the measurement of the inverter output current via the dc link sensor. Time must be allowed for the oscillation in the current to dampen sufficiently before an accurate dc link current measurement can be taken. Generally, in order to achieve a 50 Hz sinusoidal current at the inverter output, the PWM demand will also tend to be a sinusoidal waveform. This introduces complications in the dc link current sensing scheme. At low PWM demands, close to zero, the width of the dc Link conducting pulse is very narrow. As a consequence, the current pulses become increasingly dominated by the oscillation. This makes it difficult to take an accurate current measurement.

C. Effect of Deadtime

Deadtime has the effect of “cutting” into the current pulse width of the dc link current. Effectively, the duration of the conducting current is reduced, while the duration of the freewheel loop is effectively extended. Fig. 12(a) shows the freewheel period for a PWM modulation index of 0.8, with deadtime set to 1.5 μs. This may be compared to the lower trace, Fig. 12(b), which shows a waveform with the same modulation index, but with deadtime set to 2.0 μs. There is visibly a longer freewheeling period present when the deadtime is set to 2.0 μs. This enhances the time available to acquire an auto-calibration measurement. However, this is at the expense of the conducting current interval. A long deadtime adds to the difficulty of acquiring conducting loop current measurements, particularly at low PWM demands around zero.

D. Synchronization of Current

A simple mono-stable timing circuit is used to acquire both the freewheel loop and current conducting loop measurements. At the peak of the triangular carrier waveform, the PWM controller generates a single acquisition pulse, which is used as the READ pulse for the control system ADCs. Conveniently, this coincides with the optimum point for obtaining a freewheel loop measurement. The mono-stable circuit retains this READ pulse, but introduces a second READ pulse, which is delayed in relation to the first. A variable resistor enables the delay to be controlled, so the second pulse can be tuned to coincide with the optimum time to obtain a conducting loop measurement. In theory, this should coincide with the time when the PWM carrier waveform crosses zero. In practice, however, due to the imperfections caused by oscillations in the dc link current and deadtime cutting into the wave shape, the optimum position for measuring the conducting loop measurement deviates slightly. If tuned correctly, the resultant READ signal [Fig. 13(a)] will trigger the system to acquire a dc link current sensor measurement during a conducting loop and freewheel loop interval. The
ADCs trigger on the negative falling edge of each pulse in the READ signal. As shown, each READ pulse generated coincides alternately with a conducting and freewheel period in the dc link current waveform [Fig. 13(b)]. This remains the case, regardless of the pulse widths in the dc link current.

E. Inverter Output Current Reconstruction From DC Link Current Sensor Measurements

A conducting loop and freewheel loop current measurement will be acquired in every PWM cycle. These two measurements can simply be read by the controller. For the freewheel loop measurement, a set of near zero measurements will be returned to the controller as shown in Fig. 14(c). These measurements record the dc offset present in the current sensor. For the conducting loop measurement, a repetitive waveform is observed in the dc link current at twice the inverter output current frequency. As a consequence, dc link current measurements taken half an output current cycle apart are acquired with the same portion of the current sensor measurement scale. This can be utilized to advantage since, over a complete output current cycle, both the positive and negative halves of the waveform are exposed to the same current sensor nonlinearity. This produces a symmetrical nonlinearity, which will not result in a dc component in the inverter output current. At unity power factor operation, a waveform similar to that of a rectified sinusoid is recorded [Fig. 14(b)]. The freewheel loop measurement is then subtracted from the conducting loop measurement. This marks the auto-calibration stage and results in a dc offset compensated conducting loop measurement. This compensated measurement still only provides information on the magnitude of the inverter output current. Therefore, for the final stage, knowledge of the polarity of the PWM demand is important. If the PWM demand is positive, then the polarity of the conducting loop measurement is the same as the inverter output current. When the PWM demand is negative, however, the dc link conducting loop measurement is the inverse of the actual current flowing in the inverter output. Hence, the measurement is inverted. The resulting waveform is a reconstruction of the inverter output current, as shown in Fig. 14(d). It is worth noting that the sequence of events is critical to obtaining an accurate representation of the inverter output current. The compensation of the conducting loop measurement must be implemented prior to any inversion stage. If it is carried out after reconstruction of the output waveform, one half of the current cycle will be compensated for in the wrong direction. Therefore, rather than compensating for offset, an additional offset error will be introduced. To demonstrate this effect, an exaggerated example is shown in Fig. 14(e). A sudden discontinuity in the sinusoid can be seen around the zero crossing points. Generally, in practice, this discontinuity will be much smaller, but never the less it will be present in the reconstructed signal.

F. Evaluation of DC Link Current Sensing Scheme

The performance of the dc link current sensing scheme is determined via direct comparison to conventional output current inverter control. The current waveforms shown in Fig. 15 demonstrate the sinusoidal current quality at the inverter output is comparable for both control schemes. A small increase in the current total harmonic distortion (THD) is observed with the dc link current sensing scheme. Current THD is 4.11% when controlled via the output current sensor and 4.38% when controlled via the dc link current sensor. The small increase in THD level can be attributed to the difficulty in acquiring current measurements at low PWM demand. During these intervals, the dc link pulse widths are extremely narrow, making accurate current measurements increasingly difficult. As a result, a small amount of distortion is experienced in the inverter output current. Fortunately, these periods are very short since a high proportion...
of the PWM modulation range is used when controlling sinusoidal current into the mains. Furthermore, when the inverter is controlling unity power factor sinusoidal current into the grid, these periods of low PWM demand tend to coincide with low instantaneous current levels near zero. It is therefore found to be possible to let the current controller ride through these periods with only a small penalty in terms of current distortion. Further investigation into current control methods may help to overcome this issue of switching disturbance at very low PWM demands and further improve the current measurement technique. Hysteresis/bang-bang control is considered one method which may enhance the scheme, since it guarantees a minimum PWM demand and hence minimum pulse width. In this way, the controller could be adjusted to achieve a dc link current waveform which yields a current measurement that is unaffected by switching disturbance.

To test the effects of current sensor drift, the deliberate external dc offset is introduced to each current sensor in turn. The resulting dc component in the sinusoidal output current is measured via the shunt-low pass filter circuit for a range of dc offsets applied to each current sensor, the results of which are shown in Fig. 16. Control with the output current sensor has no means of accurately compensating for this offset, since it is subject to a continuous sinusoidal waveform. The dc link current sensor, however, does have the opportunity to compensate for this dc offset, since it is directly measurable during the freewheel states of the inverter. Considering manufacturers datasheet information for a range of different current sensors, the typical worst case dc offset due to drift errors is 70 mA. At 70 mA applied dc offset, the dc link current sensing scheme is capable of limiting the dc component to 8.63 mA in a 50 Hz, 10 A RMS inverter output current. This represents a 0.086% dc current component in the sinusoidal output current.

The dc link current measurement technique has been primarily developed with grid connected applications in mind. It is usual to operate these grid connected inverter systems at unity power factor with respect to the network voltage. However, the auto-calibration scheme is equally suited to other inverter applications, including systems which may operate at lower power factors. At nonunity power factor, the dc link current exhibits portions of negative current, as shown in Fig. 17. This presents no problem to the reconstruction algorithm. The rules for reconstruction remain consistent; calibration is carried out during the freewheel periods and despite the change in dc link current waveform, the polarity of the PWM demand ensures the conducting loop measurement is inverted where necessary to reconstruct the output current waveform. Furthermore, the sampled dc link waveform still repeats at twice the output current frequency, therefore ensuring symmetrical exposure to any current sensor non linearity, and thus, limiting the dc component in the output current to levels comparable with the unity power factor case.

V. CONCLUSION

This paper has considered the effect of dc offset and non-linearity errors of typical Hall Effect current sensors on the dc current component in the sinusoidal output of a grid connected inverter system. A dc link current sensing scheme, which is capable of compensating for these errors, has been proposed and experimentally tested. The results show that the proposed scheme has immunity to dc offsets in the current sensor, unlike
conventional current sensing methods. This makes it particularly applicable to grid connected, transformerless, inverter systems. This current sensing technique would also prove beneficial in transformer coupled inverter systems. The scheme would limit the dc current exposure of the coupling transformer, and help to avoid possible saturation of the transformer core. More generally, it is also applicable to other inverter topologies that utilize dc link current sensing.

REFERENCES


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