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Gate leakage mechanisms in strained Si devices

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This work investigates gate leakage mechanisms in advanced strained Si/SiGe metal-oxide-semiconductor field-effect transistor (MOSFET) devices. The impact of virtual substrate Ge content, epitaxial material quality, epitaxial layer structure, and device processing on gate oxide leakage characteristics are analyzed in detail. In state of the art MOSFETs, gate oxides are only a few nanometers thick. In order to minimize power consumption, leakage currents through the gate must be controlled. However, modifications to the energy band structure, Ge diffusion due to high temperature processing, and Si/SiGe material quality may all affect gate oxide leakage in strained Si devices. We show that at high oxide electric fields where gate leakage is dominated by Fowler-Nordheim tunneling, tensile strained Si MOSFETs exhibit lower leakage levels compared with bulk Si devices. This is a direct result of strain-induced splitting of the conduction band states. However, for device operating regimes at lower oxide electric fields Poole-Frenkel emissions contribute to strained Si gate leakage and increase with increasing virtual substrate Ge content. The emissions are shown to predominantly originate from surface roughness generating bulk oxide traps, opposed to Ge diffusion, and can be improved by introducing a high temperature anneal. Gate oxide interface trap density exhibits a dissimilar behavior and is highly sensitive to Ge atoms at the oxidizing surface, degrading with increasing thermal budget. Consequently advanced strained Si/SiGe devices are inadvertently subject to a potential tradeoff between power consumption (gate leakage current) and device reliability (gate oxide interface quality). © *2006 American Institute of Physics*. [DOI: 10.1063/1.2374191]

I. INTRODUCTION

Introducing strain into metal-oxide-semiconductor field-effect transistor (MOSFET) channels can enhance device performance through increased electron and hole mobility in tensile strained Si compared with bulk Si. Strain can be generated either globally across an entire wafer or locally through processing.[1–5] Each technique has a variety of advantages and disadvantages. Unlike local strain, global strain can increase performance in devices of conservative geometries. However, strain engineering through processing ("local strain") benefits from being relatively simple to implement. Due to the 4.2% mismatch in lattice spacing of Si and Ge atoms, tensile strain in Si can be generated through epitaxial growth of Si on a relaxed SiGe virtual substrate.[6] SiGe also plays a prominent role in local strain generation, since selective epitaxial growth of SiGe in the source/drain region can induce compressive channel strain suitable for enhancing hole mobility in *p*-MOSFET devices.[5] Consequently the impact of Ge-related processing issues has received considerable attention in recent years. In particular, there have been several reports studying the impact of Ge diffusion, since the presence of Ge can affect source/drain silicidation,[7] dopant diffusion,[8] and gate oxide quality[9] if Ge reaches the surface of the Si channel. Another challenge for globally strained Si/SiGe MOSFETs is material quality, since epitaxial growth of strained layers on relaxed virtual substrates leads to surface roughness,[10,11] which can impact photolithography in addition to gate oxide quality.[12] High quality gate dielectrics are paramount if MOSFETs with high performance and good reliability are to be realized. Ge outdiffusion from a SiGe virtual substrate or a SiGe source/drain stressor during high thermal budget processing can degrade gate oxide interface quality. This impacts MOSFET device design, since higher performance enhancements can be achieved through increasing the virtual substrate Ge composition (i.e., increasing the channel strain)[13–16] but this leads to a greater amount of Ge outdiffusion into the Si channel. Furthermore, the critical thickness of an epitaxially strained Si layer is inversely proportional to the virtual substrate Ge content. This implies that thin strained Si channels most sensitive to Ge diffusion are most stable against strain relaxation during high temperature processing. Consequently the strained Si channel thickness and virtual substrate Ge content are key design parameters for the optimizing of strained Si MOSFET devices. While several investigations have been carried out into the effects of Ge outdiffusion and epitaxial layer design on gate oxide interface quality in strained Si MOSFETs,[17–21] to date there are no comprehensive reports of gate leakage characteristics in strained Si MOSFETs. Low leakage currents are vitally important to maintain acceptable levels of power dissipation. Understanding the potential tradeoffs in device design due to gate leakage currents is therefore also necessary, especially given the literature suggesting that Si/SiGe surface roughness (which accompanies increased virtual substrate Ge compositions) plays a greater role in determining gate oxide interface trap density than Ge outdiffusion.[7,21]

Recent studies in silicon-on-insulator (SOI) structures

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have shown that energy band changes induced by mechanical tensile strain can reduce gate oxide leakage in *n*-MOSFETs[22] but the effects of Ge diffusion and surface roughness on leakage were not investigated. In this work an extensive study of gate leakage in strained Si MOSFETs is presented. Both Poole-Frenkel (PF) emission and Fowler-Nordheim (FN) tunneling mechanisms are explored and compared with theoretical predictions. A wide range of MOSFET design parameters are investigated, including virtual substrate composition, strained Si channel thickness, processing thermal budget, and complementary metal-oxide-semiconductor (CMOS) architecture. Gate leakage in both single and dual channel structures is considered. Dual channel CMOS designs comprise a surface tensile strained Si electron channel and a buried compressively strained SiGe hole channel. These structures are predicted to optimize both *n*- and *p*-channel MOSFETs on a single virtual substrate composition.[23] However, experimental results from dual channel structures is rather ambiguous, with indications that increased surface roughness and additional Ge diffusion from the buried high Ge-content structures degrades *n*-MOSFET device performance compared with performance in equivalent single channel devices.[21] Understanding the influence of the buried compressively strained SiGe layer on gate leakage is therefore imperative. The effect of virtual substrate material quality on gate leakage is also evaluated and the relative impact of each variable is discussed. Technology computer aided design (TCAD) simulations have been used to explain the experimental results. All devices were processed simultaneously and compared with bulk Si reference devices.

II. EXPERIMENTAL DETAILS

Strained Si *n*-MOSFETs were fabricated on relaxed SiGe virtual substrates using a conventional process described previously.[12] The virtual substrates were grown by low-pressure chemical vapor deposition. Devices had 6 nm thermally grown gate oxides, determined by capacitance-voltage measurements. Strained Si surface channels ranged from 4.7 to 6.0 nm in thickness, determined by transmission electron microscopy (TEM), and dual channel devices (comprising a buried compressively strained $Si_{0.75}Ge_{0.25}$ layer between the tensile strained Si surface channel and relaxed $Si_{0.85}Ge_{0.15}$ virtual substrate) were compared with single channel devices having 15%–30% Ge in the virtual substrate (Fig. 1). The impact of epitaxial material quality on gate leakage was assessed by device fabrication on virtual substrates having low (1.3 nm) and high (6.0 nm) surface roughness, measured by atomic force microscopy (AFM) on 20% Ge virtual substrates. By modifying the virtual substrate growth temperature different surface roughness values can be achieved while maintaining identical epitaxial layer structures.[24] Process thermal budget is a key factor in determining the amount of Ge diffusion that occurs in the device structures. High temperature annealing conditions can also affect gate oxide quality. A salicidation process split generated MOSFET devices both with and without silicide on the source, drains, and gate regions. Since silicide formation requires high temperature processing, the split also enabled the impact of thermal budget and annealing ambient on gate leakage to be evaluated. The additional thermal processes encountered by the salicided MOSFETs are summarized in Table I. To form gate sidewall spacers a thermal gate reoxidation stage was carried out at 800 °C for 65 min. This was followed by nitride deposition at 740 °C for 62.5 min. The sidewall spacers were subsequently anisotropically etched at low temperature using CHF_3 and Ar. To protect the surface during the following deep source/drain implants (which were performed using an implant energy of 50 keV) a further thermal reoxidation stage was carried out in dry O_2 at 800 °C for 65 min. A 15 min anneal in N_2 was performed following each thermal oxidation. Two high temperature annealing stages were carried out to form $TiSi_2$ on the gate, source, and drain regions. The first converts deposited Ti to TiSi and was carried out at 730 °C for 30 s. The second anneal transforms the high resistivity TiSi to the low resistivity $TiSi_2$ and was carried out at 850 °C for 30 s. MEDICI TCAD simulations were performed using Ge diffusion data from literature. The increased thermal budget of the salicided devices leads to increases of 0.11% and 0.43% Ge at the strained Si/SiO_2 interface (for 5.5 nm channels) using data from Ref. 25 and 26 respectively. Simulated Ge profiles using the data of Griglione *et al.*[25] are shown in Fig. 2. Gate oxide leakage was measured on MOSFET devices at room temperature using an Agilent 4155C parameter analyzer. A gate voltage was applied while the source, drain, and substrate were grounded.

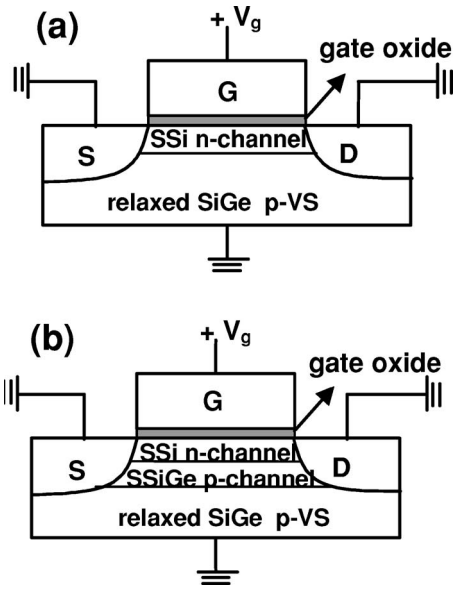

FIG. 1. MOSFET architectures: (a) single channel devices and (b) dual channel devices.

TABLE I. Extra fabrication steps for high thermal budget (salicided) devices.

Nitride spacer deposition	62.5 min, 740 °C (N_2)
×2 gate reoxidations	65.0 min, 800 °C (dry O_2) plus 15 min, 800 °C (N_2)
Silicide formation	0.5 min, 730 °C (N_2) and 0.5 min, 850 °C (N_2)

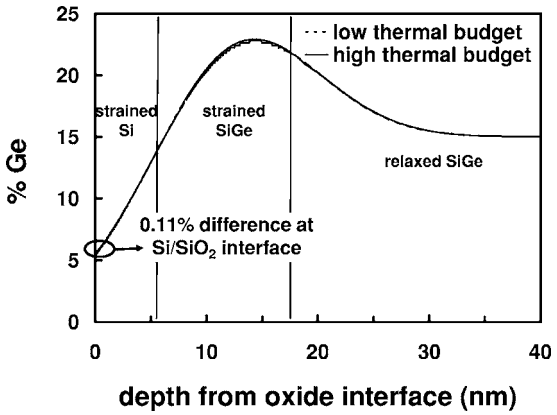

FIG. 2. MEDICI simulated Ge profiles indicating as-grown layer specification and profiles after low and high thermal budget MOSFET processes. The low thermal budget corresponds to unsalicided devices and the high thermal budget corresponds to salicided devices.

III. RESULTS AND DISCUSSION

Figure 3 shows the impact of virtual substrate Ge content on gate oxide leakage (J_g) in single channel devices measured at a gate oxide electric field E_{ox} of 11.5 MV cm^{-1}. The devices have a strained Si channel thickness of 5.5 nm and were not salicided. There is a clear decrease in leakage with increasing virtual substrate Ge composition. This is consistent with the expected FN tunneling characteristics, since increased tensile strain increases the barrier height of the strained Si/SiO_2 conduction band due to band splitting in Si. These results are in agreement with gate leakage measurements carried out by Zhao *et al.*, who used mechanical strain in SOI wafers to increase the strained Si/SiO_2 barrier height.[22] In virtual substrate MOSFETs the strained Si/SiGe conduction band offset ΔE_c is related to the virtual substrate Ge content (x) by $\Delta E_c = \sim 0.6x$ (Ref. 27) and consequently the oxide barrier height also varies, as shown in Fig. 4. The decrease in gate leakage current as the virtual substrate Ge composition increases has also been observed by Takagi *et al.*[13] These results could therefore be interpreted to imply that by using the appropriate fabrication and operating conditions strained Si may be considered as a technique for enabling low power technologies. However, at lower E_{ox} the trend with Ge content differs dramatically. Figure 5 shows that at E_{ox}=8.5 MV cm^{-1} the gate leakage becomes more degraded as the virtual substrate Ge content is increased. To

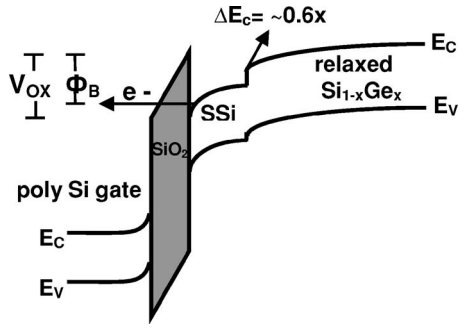

FIG. 4. Strained Si band structure when a positive gate voltage is applied.

understand the varying dependence of gate leakage on virtual substrate composition, the leakage characteristics were modeled using the extracted parameters. Figure 6 demonstrates an excellent agreement between the models and the experimental data. It is found that for the entire E_{ox} range investigated (0–13 MV cm^{-1}) FN tunneling dominates the gate leakage currents in bulk Si MOSFETs. Gate leakage current due to FN tunneling (J_{FN}) is given in Eq. (1) below,[28] where Φ_0 is the potential barrier height at the injecting interface, q is the electronic charge, h is Planck's constant, m_{Si} is the electron mass in the silicon, and m_{ox} is the effective electron mass in oxide,

$$J_{FN} = A_{FN} E_{ox}^2 \exp\left(\frac{-B\Phi_0^{3/2}}{E_{ox}}\right) \quad (1)$$

and

$$A_{FN} = \frac{q^3 (m_{Si}^*/m_{ox}^*)}{8\pi h \Phi_0}$$

and

$$B_{FN} = \frac{8\pi\sqrt{2m_{ox}^*}}{3hq}.$$

However, PF emission must be included in the model in order to fit the model to the strained Si experimental data. Since PF emission is related to oxide trapped charge, the results indicate that thermally grown oxides on strained Si/SiGe increases the bulk oxide trap density Q_{ot} compared with Si control MOSFETs. These results agree with the findings of Lee *et al.* for a much more restricted sample set.[29] Figure 5 shows that leakage in the 30% Ge devices is de-

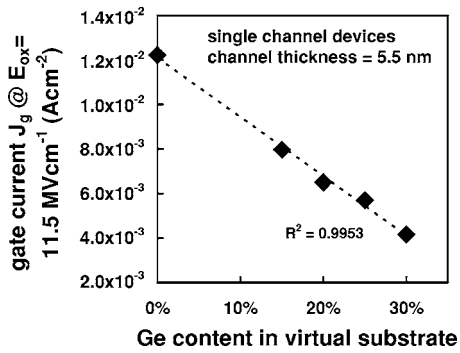

FIG. 3. Gate leakage (J_g) vs virtual substrate Ge content at a gate oxide electric field (E_{ox}) of 11.5 MV cm^{-1} (FN dominated).

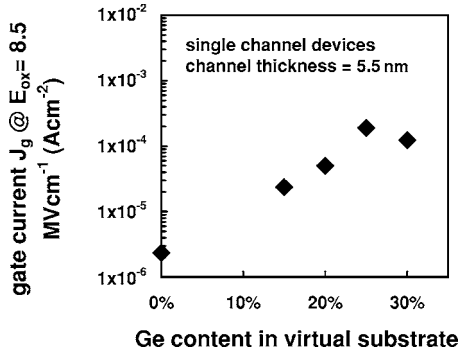

FIG. 5. Gate leakage (J_g) vs virtual substrate Ge content at a gate oxide electric field (E_{ox}) of 8.5 MV cm^{-1} (PF dominated regime).

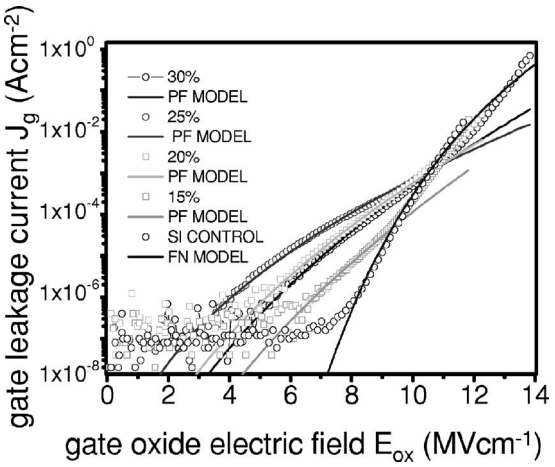

FIG. 6. Measured and modeled gate leakage characteristics for strained Si single channel *n*-MOSFETs fabricated on relaxed SiGe virtual substrates with Ge contents ranging from 0% to 30%. MOSFETs have 5.5 nm strained Si channel thicknesses.

creased compared with leakage in the 25% Ge devices, indicating that PF emission decreases as the virtual substrate Ge content is increased above 25%. There is a significant increase in strained Si MOSFET gate oxide interface trap density (D_{it}) observed when the virtual substrate Ge composition exceeds 25% Ge.[7,15,30] It is possible that large number of interface states in the 30% Ge MOSFETs act to trap electrons.[31] This would decreases the number of free electrons tunneling towards the gate and result in reduced PF leakage.

Bulk oxide traps in strained Si devices can originate from a number of sources. Ge outdiffusion from the virtual substrate degrades both gate oxide interface trap density and fixed charge,[15,20,30] thus it is plausible that Q_{ot} may also be affected. Figure 7 shows the impact of strained Si channel

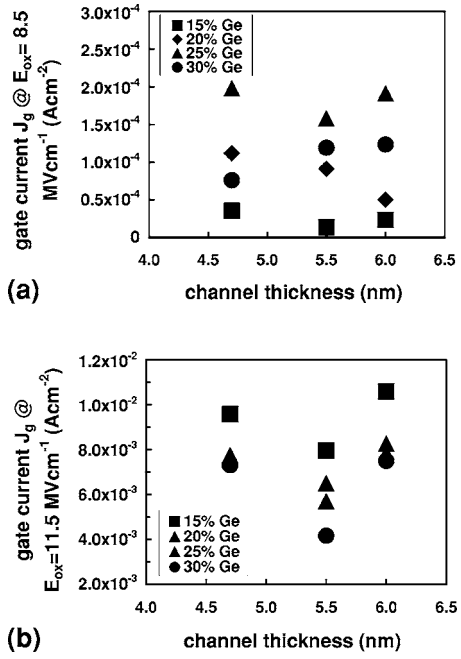

FIG. 7. Impact of strained Si channel thickness on (a) PF emission and (b) FN leakage in single channel *n*-MOSFETs.

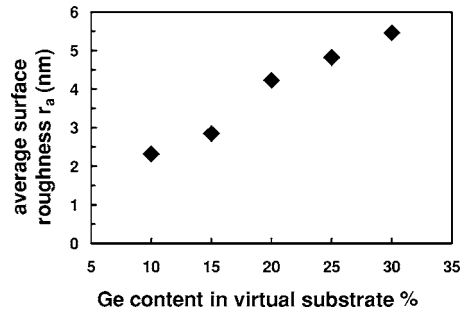

FIG. 8. Surface roughness vs virtual substrate Ge content measured by AFM.

thickness on gate leakage current. In both PF emission [Fig. 7(a), E_{ox}=8.5 MV cm^{-1}] and FN tunneling [Fig. 7(b), E_{ox} =11.5 MV cm^{-1}] regimes there is little impact of channel thickness on gate leakage. Since more Ge atoms reach the strained Si/oxide interface in thinner channels, Ge outdiffusion cannot be considered a dominating factor in PF emission. This markedly contrasts with D_{it} measurements for these devices, which increased by more than one order of magnitude when the channel thickness is varied by the same amount.[20]

Surface roughness can also increase Q_{ot} since it affects the structural formation of the gate oxide, leading to unsatisfied dangling bonds. Roughness measurements were performed on the device wafers using AFM and confirmed that surface roughness is increased as the virtual substrate Ge content is increased (Fig. 8). The higher surface roughness of the MOSFETs fabricated with higher levels of strain may therefore contribute to the higher PF emission observed (Fig. 5). The role of surface roughness on PF leakage was confirmed through leakage measurements in MOSFET devices having identical dual-channel layer structures and material compositions but differing surface roughness values. This was possible by modifying the virtual substrate growth conditions. Figure 9 shows that MOSFETs having higher surface roughness exhibit increased leakage compared with MOSFETs having lower surface roughness. For this experiment devices were fabricated both with and without the salicide process, creating "high" and "low" thermal budgets. Modeling reveals that at low E_{ox} the low thermal budget devices

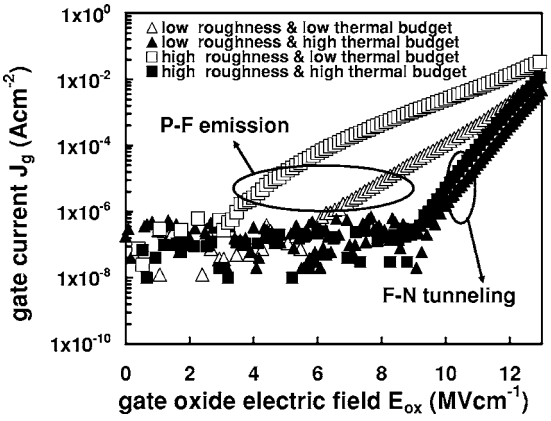

FIG. 9. Gate leakage (J_g) characteristics for dual channel strained Si *n*-MOSFETs.

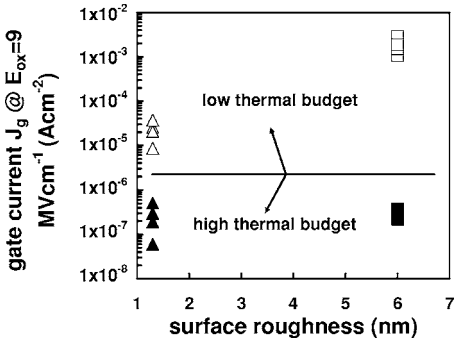

FIG. 10. Impact of thermal budget and epitaxial surface roughness on gate leakage (J_g) at an oxide electric field (E_{ox}) of 9 MV cm^{-1}.

experience an additional leakage component due to P-F emissions. However, the high thermal budget devices exhibit typical FN dominated leakage characteristics throughout the entire E_{ox} range investigated, without any evidence of P-F emissions. This explains why there is a greater dependence of gate leakage on surface roughness for the low thermal budget devices (Fig. 10).

Using the method of Hill and Coleman[32] D_{it} was measured on all four sets of dual-channel devices (low/high thermal budget, low/high surface roughness). For the high thermal budget devices, the increase in surface Ge concentration from the additional silicide thermal budget (Fig. 2) causes a significant increase in D_{it} (data not shown). Moreover, the difference in thermal budget experienced by the salicided and unsalicided devices was found to have a greater impact on D_{it} than the difference in surface roughness values between the wafers. This contrasts with the findings for gate leakage presented above. The high sensitivity of D_{it} to Ge outdiffusion is consistent with previous reports.[17–20]

The improved leakage characteristics in the high thermal budget devices can be explained by the extra N_2 annealing encountered during the salicidation processes. In particular, the ~1 h nitride deposition step used for sidewall spacers, the high temperature rapid thermal annealing (RTA) stages carried out during the silicide formation steps, and the anneals carried out following the extra thermal oxidations act to anneal out the bulk gate oxide traps. Consequently the dominating leakage mechanism changes from PF emission to FN tunneling following salicidation. In conventional MOSFET devices a low temperature forming gas anneal (approximately 10% H_2 in N_2) is commonly used to improve gate oxide trap density prior to final passivation. Alternatively a higher temperature anneal is carried out directly after the gate oxidation stage.[33] Introducing forming gas anneals has also been shown to improve gate leakage in thermal oxides grown on strained Si.[19] Since all devices in the current study already received a 30 min H_2/N_2 anneal this work demonstrates that additional nitrogen anneals should be employed to improve gate leakage characteristics further in strained Si devices. However, since gate oxide interface trap density becomes degraded with increasing thermal budget and gate leakage has been shown to improve with increasing thermal budget, this study also identifies an important tradeoff between D_{it} and Q_{ot} for strained Si MOSFETs.

IV. SUMMARY

A systematic study of gate leakage mechanisms in tensile strained Si MOSFETs has been carried out. Devices were simultaneously fabricated using a range of virtual substrate alloy compositions, strained Si channel thicknesses, epitaxial material quality, and CMOS layer architectures. A process split further enabled the impact of thermal annealing on leakage in strained Si MOSFETs to be analyzed. The wide parameter space investigated has provided significant insight into the fundamental mechanisms governing gate leakage in strained Si MOSFETs. At high E_{ox} where gate leakage is dominated by FN tunneling, tensile strained Si MOSFETs were found to exhibit lower leakage levels compared with bulk Si devices. This is a direct result of strain-induced splitting of the conduction band states. However, at lower E_{ox} PF emission contributes to strained Si gate leakage and increases with increasing virtual substrate Ge content. It has been demonstrated that the PF emission is predominantly caused by surface roughness generating bulk oxide traps, opposed to Ge diffusion. This contrasts gate oxide interface trap density which is highly sensitive to Ge atoms at the oxidizing surface. Introducing a high temperature N_2 anneal modifies the leakage characteristics at low E_{ox} by reducing PF emissions and enables typical FN tunneling characteristics to be restored. Consequently, the sensitivity of gate leakage on surface roughness in strained Si MOSFETs can be reduced by careful process optimization.

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