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Top-down fabrication of single crystal silicon nanowire using optical lithography

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A method for fabricating single crystal silicon nanowires is presented using top-down optical lithography and anisotropic etching. Wire diameters as small as 10 nm are demonstrated using silicon on insulator substrates. Structural characterization confirms that wires are straight, have a triangular cross section and are without breakages over lengths of tens of microns. Electrical characterization indicates bulk like mobility values, not strongly influenced by surface scattering or quantum confinement. Processing is compatible with conventional silicon technology having much larger critical dimensions. Integrating such nanowires with a mature CMOS technology offers an inexpensive route to their exploitation as sensors. © 2012 American Institute of Physics. [<http://dx.doi.org/10.1063/1.4737463>]

I. INTRODUCTION

Silicon nanowires (SiNWs) having nm-scale cross-sections and μm -scale lengths are ideal for sensor applications, where their large surface to volume ratio can be exploited. Furthermore, they can be directly integrated with either CMOS or thin film System-on-Panels technologies.¹ The electrical detection of bio-molecules is a very attractive prospective application, because it allows the integration of biosensors with CMOS, which could leverage nanosensor array systems for fast, high throughput analysis of biological processes. Such systems could revolutionise many areas in medicine and biochemistry, such as the detection and diagnosis of diseases and the development of new drug delivery systems. However, the CMOS technology required for such applications does not demand even sub-100 nm critical dimensions and mature technologies could do the job satisfactorily in many cases at low cost. There is therefore a need for inexpensive nanowire fabrication, without the use of advanced lithography.

The realization of SiNWs has been demonstrated by several methods but there is no preferred technique. Bottom up growth of nanowires from seeds forms vertical wires.^{2–4} Typically, vapour liquid solid (VLS) growth is employed, using metallic nanoclusters such as gold (Au) as the nucleation site. The size of the metal catalyst determines the diameter of the nanowire. However, the potential for metal contamination is a concern when this method is used. The uncontrolled growth orientation and position of the wires make it difficult for this approach to be used for transistor or sensor applications. Top-down patterning gives lateral SiNWs with very well defined size and location.^{5–7} Although this approach provides a more compatible MOSFET-based platform, its complexity is also increased as it generally relies on patterning methods using expensive high resolution lithography.

Experiments performed by Ciucci *et al.*⁸ and Pennelli *et al.*⁹ made use of silicon on insulator (SOI) as a starting substrate. The formation of the Si nanowire was performed by anisotropic etching using potassium hydroxide (KOH). However, the patterning in order to locate the nanowires was achieved using electron beam (e-beam) lithography, which is not suitable for high-volume manufacturing because of its limited throughput. The use of conventional optical lithography to fabricate silicon nanowires using SOI has also been considered by a number of authors.^{10–12} However, the nanowires obtained were wider than the nanowires produced using e-beam lithography. A series of complex size reduction processes, such as etching and oxidation, were necessary in order to obtain small nanowire dimensions. Another approach is to deposit silicon over a sacrificial layer such as SiO₂ and then use an anisotropic (vertical) etch to create an amorphous silicon nanowire, similar to the formation of a sidewall spacer in MOSFET technology.^{13,14} This approach requires further annealing to transform the amorphous Si nanowire into poly-crystalline silicon.

In this paper we report a method for fabricating single crystal silicon nanowires using top-down optical lithography, together with simple oxidation and anisotropic etching using KOH. Wire diameters as small as 10 nm are demonstrated on SOI substrates. In Sec. II, the fabrication is described, while Sec. III presents our results. The work is discussed in Sec. IV and summarized in Sec. V.

II. FABRICATION OF SILICON NANOWIRE

Silicon nanowires were fabricated from SOI substrates, where the buried oxide (BOX) was 400 nm thick. The silicon top layer was 145 nm thick and doped n-type (phosphorous) to a concentration of $2 \times 10^{18} \text{ cm}^{-3}$. A layer of silicon nitride (Si₃N₄) of thickness 60 nm is deposited using plasma-enhanced chemical vapor deposition (PECVD) to act as

mask for subsequent KOH etching. It is then patterned using optical lithography and etched using buffered oxide etch (BOE) solution to expose a region of the silicon top layer (Fig. 1(a)). The first KOH etch process (45% in weight at 50 °C) is performed. The exposed silicon is etched preferentially in the Si $\langle 100 \rangle$ plane, which produces a sidewall angle of 54.7° to the horizontal surface and exposes a $\langle 111 \rangle$ silicon sidewall plane, as shown in Fig. 1(b). After the etching process, the resulting Si $\langle 111 \rangle$ plane is thermally oxidized (Fig. 1(c)). It is anticipated that this oxidation step also improves the surface roughness of the exposed Si $\langle 111 \rangle$ surface. The Si_3N_4 layer is then removed via wet etching using boiling phosphoric acid (Fig. 1(d)). The SiO_2 layer formed over the Si $\langle 111 \rangle$ plane during thermal oxidation then acts as a mask for a further KOH etch. This second KOH etch exposes the other diagonal Si $\langle 111 \rangle$ side (Fig. 1(e)) and completes the triangular nanowire. The SiO_2 mask is removed using BOE leaving the structure shown schematically in Fig. 1(f). Further etching can remove the BOX to leave a free standing nanowire. A layer of SiO_2 is then deposited to provide isolation for the Si nanowires. This layer is then patterned to create contact windows. Contact metallization of the Si nanowires was performed using a stack of Ti (80 nm)/Al (70 nm) and the samples were annealed in a forming gas (H_2/N_2) ambient at 500 °C for 2 min.

The oxide mask produced by thermal oxidation of the Si $\langle 111 \rangle$ plane self aligns to define the nanowire structure without the need for an additional patterning step. The nanowire

location is defined by the optical lithography mask edge. The quality of the Si_3N_4 mask edge is controlled by optimising the pre and post bake temperatures of the photoresist and the developing time. This is crucial for reducing the line edge roughness (LER) of the Si nanowire sidewall surface as the etching process proceeds. Fig. 2 shows the edge profile of the Si surface after the first KOH etch using atomic force microscopy (AFM). The edge roughness (root mean square average, R_q) was observed to vary from 6.48 nm to 1.78 nm depending on photoresist treatment, demonstrating the importance of careful control during the lithographic step to produce nanowires with minimal LER.

III. RESULTS

Structural characterization was performed on Si nanowires that were fabricated using the process described in Sec. II. The nanowire cross section is determined by the thickness of the silicon layer on top of the BOX, together with the oxidation and KOH etch conditions. The nanowire length is determined directly from the lithography mask design. Continuous nanowires were fabricated of length 1–20 μm . Fig. 3(a) shows the top view of the fabricated Si nanowire obtained using a scanning electron microscope (SEM). A continuous straight Si nanowire can be seen clearly on top of the BOX. To obtain the images in Fig. 3(b), the samples were tilted at an angle of 30° in order to inspect the profile on both $\langle 111 \rangle$ Si faces of the nanowire.

FIG. 1. Schematic illustration of the top-down approach to fabricating silicon nanowires by optical lithography with oxidation and anisotropic etching.

FIG. 2. AFM profiles illustrating the impact of photoresist treatment on nanowire LER after the KOH etching: (a) a rough $\langle 111 \rangle$ Si sidewall where RMS roughness $R_q = 6.48 \text{ nm}$ and (b) a smooth $\langle 111 \rangle$ Si sidewall where $R_q = 1.78 \text{ nm}$.

Side A corresponds with the Si $\langle 111 \rangle$ plane revealed from the first KOH etch, while side B corresponds with the Si $\langle 111 \rangle$ plane revealed from the final KOH etch. It is observed that both sidewalls of the Si nanowire are smooth, indicating minimal LER, consistent with the AFM data of Fig. 2.

The cross section profiles of the nanowires were obtained by focused ion-beam (FIB) milling and again using the SEM to image, as shown in Fig. 4. The nanowire cross section is observed to be triangular. This is due to the preferential etching of KOH along Si $\langle 100 \rangle$ planes, which reveals Si $\langle 111 \rangle$ surfaces. The angle between the Si $\langle 111 \rangle$ plane and

FIG. 3. (a) SEM image showing a top view of the fabricated silicon nanowire. (b) SEM images showing the smooth $\langle 111 \rangle$ Si sidewalls for each side of the silicon nanowire following KOH etching.

FIG. 4. SEM image of a Si nanowire cross section, as revealed by FIB milling.

the Si $\langle 100 \rangle$ plane is measured as 57.1° , which is in good agreement with the theoretical value of 54.7° . The height of the nanowire is 68 nm and the width is 88 nm, corresponding to a cross sectional area of approximately 3000 nm^2 .

Current-voltage (I-V) measurements were conducted to confirm that the nanowires were electrically continuous and that an ohmic contact had been established between the deposited metal stack and the highly doped n-type Si nanowires. Using a Si nanowire of length, $L_{\text{NW}} = 17.5 \mu\text{m}$, the results shown in Fig. 5 indicate that nanowires are electrically continuous and that an ohmic characteristic is achieved. The electrical data in Fig. 5 includes resistance contributions for the nanowire and contact resistance. In order to deconvolve these contributions, four-point probe measurements were carried out. These measurements revealed a nanowire resistance of $1.5 \text{ M}\Omega$, which is equivalent to a nanowire resistivity of $0.025 \Omega \text{ cm}^{-1}$. This shows that the Si nanowire doping concentration is comparable to the initial phosphorus doped silicon layer on top of the BOX ($2 \times 10^{18} \text{ cm}^{-3}$).

IV. DISCUSSION

It has been observed previously that carrier mobility can be reduced in Si nanowires due to surface scattering.¹⁵ However, this is usually limited to very thin nanowires which are smaller than $5 \text{ nm} \times 5 \text{ nm}$,¹⁶ which is a thickness comparable to the inversion layer in a MOSFET and where transport is

FIG. 5. I-V characteristic for a silicon nanowire with $L_{\text{NW}} = 17.5 \mu\text{m}$, exhibiting ohmic behaviour.

dominated by surface scattering when surface electric fields are applied.¹⁷ The cross sectional area of the Si nanowires, whose electrical properties are shown in Fig. 5 are significantly larger than 5 nm and no surface electric field is intentionally applied. So the effect of surface scattering is expected to be negligible and the mobility of carriers affected mainly by the influence of impurity scattering.

The effective mobility of electrons, μ_e , in the silicon nanowires was obtained from the four point probe resistance, R , and determined from Eq. (1):

$$R = \frac{L_{NW}}{n\mu_e qA}. \quad (1)$$

This result can now be compared with the bulk Si mobility that can be calculated using the Caughey-Thomas expression for mobility in Eq. (2):

$$\mu_e \equiv \mu_{\min} + \frac{\mu_L - \mu_{\min}}{1 + \left(\frac{N_{\text{imp}}}{N_{\text{ref}}}\right)^\alpha}, \quad (2)$$

where $\alpha = 0.72$, $\mu_{\min} = 65 \text{ cm}^2/\text{Vs}$, $\mu_L = 1330 \text{ cm}^2/\text{Vs}$, $N_{\text{ref}} = 8.5 \times 10^{16} \text{ cm}^{-3}$, and N_{imp} is the concentration of dopant.¹⁸ The effective mobility, μ_e , is calculated from Eq. (2) to be $242 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$. This result compares well with the bulk electron mobility for Si doped at $2 \times 10^{18} \text{ cm}^{-3}$, the same concentration as the starting Si layer above the BOX, which is $248 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$. This confirms that these Si nanowires have a sufficiently large cross section that surface scattering and quantum-confinement effects are negligible. For comparison purpose, Si nanowires prepared using superlattice nanowire pattern transfer¹⁹ reported an effective mobility of $100 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ for carriers in boron doped Si nanowires (10^{18} cm^{-3}) having dimensions of $30 \text{ nm} \times 17 \text{ nm}$, which is close to the mobility in the equivalent bulk Si. Vaurette *et al.*²⁰ have also concluded that for thicknesses and widths of nanowires that are well above 10 nm, confinement effects will not be observable.

The repeatability and yield of silicon nanowires fabricated using this technique have been investigated. It was found that for SOI substrates having a Si top layer thickness of more than 50 nm, the nanowires are fabricated consistently with near 100% yields. However, it is more challenging to obtain a continuous nanowire structure using SOI substrates with a thinner Si top layer, because they will lead to nanowires having a smaller cross sectional area. For these thinner nanowires, the process window for oxide growth and etching is more limited. Common issues faced include failure of the SiO_2 to act as a mask for the final KOH etching, resulting in discontinuities along the length of the silicon nanowire. The thicknesses of Si_3N_4 and the thermally grown SiO_2 on the first exposed Si $\langle 111 \rangle$ plane are also critical and if the etch rate during the final KOH etch is too rapid, it can result in Si being over-etched. Thus a slower etch rate for the final KOH etch is required, which can be achieved by using a lower etching temperature.

Thin silicon nanowires were fabricated using SOI wafers having a silicon thickness of 25 nm above the BOX. The

wafer was again masked with a 60 nm silicon nitride and patterned using optical lithography. The process followed the schematic process flow shown in Fig. 1. The final KOH etch was performed at a temperature of 30°C , which reduces the etch rate by 75% compared with the previous nanowire processing, as discussed in Sec. II, where the KOH etch was carried out at 50°C .

The resulting samples were scanned using AFM after the final SiO_2 removal and no discontinuity or breakage along the nanowire length of up to $10 \mu\text{m}$ was observed. It was not possible to get useful cross sectional images from SEM as the dimensions were too small. Cross-section foils for transmission electron microscopy (TEM) were prepared using an FEI Helios FIB microscope. The samples were examined in a JEOL 2100F FEG TEM operating at 200 kV. Fig. 6(a) shows a low-magnification TEM image of the Si-nanowire (circled) which is surrounded by the Pt deposit used to protect the specimen during FIB preparation of thin TEM cross-sections. The dimensions of the nanowire are observed to be approximately 10 nm in both height and width, corresponding to a cross sectional area of around 50 nm^2 . A phase contrast image is shown in Fig. 6(b) with the crystal structure of the nanowire resolved. From the fast Fourier transform of the image around the nanowire region (figure inset) the nanowire axis is determined to be along $[110]$. Furthermore, the nanowire is bounded by $(\bar{1}11)$, $(1\bar{1}1)$, and (002) crystal faces. The boundaries of the nanowire are not sharp which could be

FIG. 6. (a) Low-magnification TEM image of the Si-nanowire (circled) surrounded by the Pt deposit used to protect the sample during FIB preparation; (b) phase contrast image showing the crystal structure of the nanowire. The fast Fourier transform of the nanowire region is shown in the inset and corresponds to a $[110]$ crystallographic direction.

due to the nanowire not being perfectly straight through the TEM foil thickness.

V. CONCLUSION

A top down approach using optical lithography has been shown to fabricate single crystal Si nanowires with dimensions down to 50 nm². The fabrication process utilizes the lithography mask edge combined with KOH etching and oxidation, resulting in a self aligned process that requires no high resolution lithography. An SOI substrate has been used as a convenient etch stop, but conceivably this could be eliminated by the use of an isotropic etch following the KOH etching. The conductivity of larger nanowires, as determined by four point probe measurement, is ohmic and is of the same magnitude as the bulk conductivity of the silicon layer above the BOX on the SOI substrate used to fabricate the nanowires. Thus, the conductivity is not influenced by factors such as quantum confinement or surface scattering at these dimensions. To achieve the smallest dimensions using this approach, great care is required, while the process window for oxidation and etching becomes more narrow.

The work shows that good quality silicon nanowires can be fabricated using techniques that are compatible with mature CMOS technologies. This offers the prospect of low cost applications of nanowires, for example, exploiting their large surface to volume ratio in sensor applications.

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- ¹Z. Li, Y. Chen, X. Li, T. I. Kamins, K. Nauka, and R. S. Williams, *Nano Lett.* **4**, 245 (2004).
- ²W. Lu and C. Lieber, *Nat. Mater.* **6**, 841 (2007).
- ³A. Greytak, L. Lauhon, M. Gudixsen, and C. Lieber, *Appl. Phys. Lett.* **84**, 4176 (2004).
- ⁴M. Bjork, B. Ohlsson, C. Thelander, A. Persson, K. Deppert, L. Wallenberg, and L. Samuelson, *Appl. Phys. Lett.* **81**, 4458 (2002).
- ⁵H. I. Liu, D. K. Biegelsen, F. A. Ponce, N. M. Johnson, and R. F. W. Pease, *Appl. Phys. Lett.* **64**, 1383 (1994).
- ⁶Y. Nakajima, Y. Takahashi, S. Horiguchi, K. Iwadate, H. Namatsu, K. Kurihara, and M. Tabe, *Appl. Phys. Lett.* **65**, 2833 (1994).
- ⁷A. Potts, D. G. Hasko, J. R. A. Cleaver, and H. Ahmed, *Appl. Phys. Lett.* **52**, 834 (1988).
- ⁸S. Ciucci, F. D'Angelo, A. Diligenti, B. Pellegrini, G. Pennelli, and M. Piotta, *Microelectr. Eng.* **78–79**, 338 (2005).
- ⁹G. Pennelli and M. Piotta, *J. Appl. Phys.* **100**, 054507 (2006).
- ¹⁰P. Bruschi, A. Diligenti, and M. Piotta, *Microelectr. Eng.* **57–58**, 959 (2001).
- ¹¹Y. K. Choi, J. Zhu, J. Grunes, J. Bokor, and G. A. Somorjai, *J. Phys. Chem. B* **107**, 3340 (2003).
- ¹²K. N. Lee, S. W. Jung, W. H. Kim, M. H. Lee, W. K. Seong, M. Kim, and Y. S. Lee, in *5th IEEE Conference on Sensors* (2006), p. 1269.
- ¹³F. Demami, L. Pichon, R. Rogel, and A. C. Salaün, *IOP Conf. Ser.: Mater. Sci. Eng.* **6**, 012014 (2011).
- ¹⁴K. Sun, M. M. A. Hakim, and P. Ashburn, *Electrochem. Solid-State Lett.* **15**, H62 (2012).
- ¹⁵V. Schmidt, J. V. Wittemann, S. Senz, and U. Goesele, *Adv. Mater.* **21**, 2681 (2009).
- ¹⁶E. B. Ramayya, D. Vasileska, S. M. Goodnick, and I. Knezevic, *J. Appl. Phys.* **104**, 063711 (2008).
- ¹⁷S. Takagi, A. Toriumi, M. Iwase, and H. Tango, *IEEE Trans. Electron Devices* **41**, 2357 (1994).
- ¹⁸D. M. Caughey and R. E. Thomas, *Proc. IEEE* **55**, 2192 (1967).
- ¹⁹D. W. Wang, B. A. Sheriff, and J. R. Heath, *Nano Lett.* **6**, 1096 (2006).
- ²⁰F. Vaurette, J. P. Nys, D. Deresmes, B. Grandidier, and D. Stievenard, *J. Vac. Sci. Technol. B* **26**, 945 (2008).