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Pre-threshold Voltage as a Low Component Count Temperature Sensitive Electrical Parameter without Self-Heating

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Abstract — Temperature Sensitive Electrical Parameters (TSEPs) are promising for measurement of the IGBT junction temperature. Many TSEPs have been proposed in the literature and most require current sensors, and convoluted hardware and data processing, which are associated with increased complexity and cost. In this letter, a new TSEP is proposed called pre-threshold TSEP, $V_{GE(pre-th)}$. $V_{GE(pre-th)}$ requires only a voltage sensor and a counter. Besides less hardware requirement, $V_{GE(pre-th)}$ does not suffer from self-heating – a problem that most TSEPs encounter. This letter presents the operation of $V_{GE(pre-th)}$ with the help of simulation. Experimental tests on a 3.3kV, 800A IGBT were conducted to characterize $V_{GE(pre-th)}$. It is shown that the new TSEP proposed has a sensitivity of $-2.2\text{mV}/^\circ\text{C}$.

Index Terms — Insulated Gate Bipolar Transistor (IGBT), Health Monitoring, TSEP, Junction Temperature, Threshold Voltage.

I. INTRODUCTION

IGBTs generate heat due to power dissipation owing to the concurrency of voltage and current in the IGBT switching and conduction states. Traditionally, in an IGBT cell, the junction region has often been reported as the hottest region [1], thus the term junction temperature T_j has commonly been used when referring to an IGBT device/chip temperature. In practice, however, the hottest point of an IGBT chip depends on load conditions and semiconductor technology used [2]. In multi-chip power devices the terminology virtual junction temperature T_{vj} is often used and defined by Infineon and Hitachi in their applications notes [3, 4].

In order to extract T_{vj} thermal-electric models can be employed in power electronics converters estimating T_{vj} from a temperature sensor adhered to the baseplate/heatsink [5]. It is well known that the estimated error of T_{vj} becomes smaller when using a more detailed and therefore complex model [6, 7] to the expense of required computational resources. Another technique to obtain T_{vj} is to make use of Temperature Sensitive Electrical Parameters (TSEPs). Over the last two decades many TSEPs have been proposed which are summarized in Table I. TSEPs can be split into two groups: self-heating TSEP and non-self-heating TSEP (shown with * in Table I). A self-heating TSEP measures the temperature at a time when current flows through the collector either when the collector current rises or falls during switching, or when it is nearly constant during on-state mode. A non-self-heating TSEP measures at a time where no current flows through the collector. Non-self-heating TSEPs

give a better temperature indication as it detects T_{vj} immediately prior a switching event or very shortly after a switching event. Table I also shows the number and type of required sensors (voltage/current) and sensor functions. “Read” is a sensor to determine the measured temperature and “Trigger” is a sensor to capture an event that triggers the read sensor. Beside the sensors listed in Table I many self-heated TSEPs require additional sensors. These sensors are used to determine if the same operational conditions for IGBT health monitoring are met. Either existing converter sensors like phase current sensors or dc-link voltage sensors can be used or additional sensors must be added. Sensors that determine the operational conditions of IGBTs are not shown in Table I.

Any circuit added to a power converter must be small, lightweight and of low cost. This is also applicable to the TSEP measurement circuit. Voltage sensors are simpler and lightweight compared to current sensors, and in general current based TSEPs (Table I) are not preferred from a practical perspective. The measurement of $V_{CE(sat)}$ and dV_{CE}/dt requires voltage sensors connected between collector and emitter terminals. The sensor must deal with large voltage swings ranging between hundreds of volts (blocking stage) and few volts of on-state drop (saturation voltages). In order to protect the measurement circuit from high voltages additional hardware must be added as described in [8], which leads to increased hardware complexity. t_{don} and t_{doff} TSEPs are not favorable as they are commonly short approximately several hundreds of nanoseconds depending on the switching performance and load current.

Excluding t_{don} , t_{doff} , current based TSEPs, $V_{CE(sat)}$ and dV_{CE}/dt from Table I, $V_{GE(Miller)}$ and $t_{GE(Miller)}$ (time is normally in a fraction of tens of nanoseconds) are preferable TSEPs, but both of these TSEPs require the fast capture of a large set of data over a given period (i.e. the length of Miller plateau). Data must then be processed which requires specific software algorithms.

TABLE I
ONLINE IGBT TSEPS

TSEP	Required Sensor(s)	Sensor Function	Ref.
Turn-on delay time ($t_{d(on)}$)	{ voltage current +	trigger trigger	[9]
Turn-off delay time ($t_{d(off)}$)	{ voltage current +	trigger trigger	[9]
Miller plateau voltage level ($V_{GE(Miller)}$)	voltage	read	[10]
Miller Plateau width ($t_{GE(Miller)}$)	{ voltage voltage	trigger read	[11]
Threshold voltage ($V_{GE(th)}$)	{ voltage current +	read trigger	[12]
*Gate peak current ($I_{G(peak)}$)	current +	read	[13]
Saturation voltage ($V_{CE(sat)}$)	voltage	read	[14]
Collector-Emitter slope (dV_{CE}/dt)	voltage	read	[11]
Collector current slope (dI_C/dt)	current	read	[9]
Collector tail current ($I_{C(tail)}$)	current	read	[10]
Collector peak current ($I_{C(peak)}$)	current	read	[9]
Collector saturation current ($I_{C(sat)}$)	current	read	[15]
*Collector leakage current ($I_{C(leak)}$)	current	read	[16]

trigger: sensor is used to trigger an event

read: sensor is used to read a measured value

All current sensors measure collector currents except + which measure gate current

This letter proposes a TSEP that neither requires a current sensor or complex hardware to monitor the collector emitter voltage nor does it require any processing algorithms to extract data. The proposed TSEP obtains information from the gate emitter voltage waveform V_{GE} during turn-on. Measurement is made slightly before $V_{GE(th)}$ is reached. The TSEP is therefore called pre-threshold voltage $V_{GE(pre-th)}$. This TSEP is based on the temperature dependency of $V_{GE(th)}$. V_{GE} starts always from a fixed voltage level and as $V_{GE(th)}$ changes with temperature the gradient of the V_{GE} waveform will change with temperature. Thus any point along V_{GE} can be used as TSEP. This knowledge allows the use of a simple counter that determines the point of measurement rather using a current sensor to determine when to measure. The counter will be triggered by the PWM signal to synchronize the measurement. Besides low hardware requirement, the utilization of $V_{GE(pre-th)}$ has the advantage that at this point the collector current has not started to flow through the device thus $V_{GE(pre-th)}$ is a non-self-heating TSEP. All TSEPs in Table I are self-heating TSEPs except $I_{C(leak)}$ and $I_{G(peak)}$ which however require current sensors.

II. PRE-THRESHOLD VOLTAGE AS TSEP

The MOS structure of the IGBT gate comprises inherent capacitances (C_{GE} , C_{GC} and C_{CE}) and the internal temperature dependent gate resistance $R_{Gint}(T)$. The input capacitances C_{GE} and C_{GC} need charging via an external gate resistor R_{Gext} . R_{Gext} , $R_{Gint}(T)$, C_{GE} and C_{GC} form an RC circuit with the gate supply voltage V_{GG} . V_{GE} has the shape of an exponential function during the turn-on process starting from the PWM signal T_0 until $V_{GE(th)}$. Fig. 1 shows the principal MOS structure connected to V_{GG} and shows the principal V_{GE} waveform from the PWM trigger point T_0 to $V_{GE(th)}$ which depends on the chip temperature.

Fig. 1. RC circuit forming the waveform of V_{GE} from the PWM trigger event T_0 to $V_{GE(th)}$ during turn-on.

The V_{GE} waveform can be given as,

$$V_{GE} = (V_{GE(th)} + 10V)(1 - e^{-t/(R_{Gint}(T)(C_{GE} + C_{GC}))}) - 10V \quad (1)$$

Eq. (1) shows that V_{GE} is a function of R_{Gint} which is temperature dependent therefore R_{Gint} varies the gradient of the V_{GE} waveform. Consequently when measuring at a fixed point of time the voltage level changes with temperature and this effect can be used as TSEP which is named pre-threshold gate emitter voltage $V_{GE(pre-th)}$.

III. SIMULATION RESULTS

A 3.3kV, 800A IGBT power module DIM800NSM33-F, from Dynex Semiconductor was chosen as the reference module, used in the simulations and experimentation. The DIM800NSM33-F IGBT is a sixth generation trench gate soft punch-through IGBT. A simulation model derived from the datasheet was realized using SaberRD. The developed model included a dynamic electro-thermal model which calculates T_{vj} from a given thermal impedance and a thermal pin that represents the case temperature which can be defined as input as shown in Fig. 2. Prior start of the simulation SaberRD sets T_{vj} to the defined case temperature ($T_{vj}=T_c$). This way, T_{vj} can be varied by changing T_c at the start of the simulation.

Fig. 2. IGBT-TSEP characterization circuit implemented in SaberRD for turn on.

The double pulse tester shown in Fig. 2 was only simulated for one single impulse in order to establish the relation between T_{vj} and $V_{GE(pre-th)}$. The V_{GE} turn-on period is shown in Fig. 3 at different temperatures. A gate resistor of 3.9Ω for turn-on was used between the ideal pulsed voltage generator and the gate of the IGBT. The voltage V_{GE} changes from -10V which is OFF to +15V which is ON. Fig. 3 shows that the gate emitter voltage waveform V_{GE} is rising towards $V_{GE(th)}$. As $V_{GE(th)}$ changes its value with respect to time as a function of temperature the slope of V_{GE} changes, and therefore the voltage level $V_{GE(pre-th)}$ which is measured at a fixed time changes with respect to temperature. Fig. 3 shows a discrepancy between all

three voltage waveforms between $0.04\mu\text{s}$ and $0.08\mu\text{s}$; above $0.08\mu\text{s}$ is $V_{GE(th)}$. $V_{GE(pre-th)}$ measurement at $0.06\mu\text{s}$ results in 2.5V, 3.1V and 3.6V at 100°C , 60°C and 20°C respectively.

Fig. 3. SabeRD illustration of V_{GE} measurements at 20°C , 60°C and 100°C .

IV. CHARACTERIZATION OF $V_{GE(pre-th)}$

A high voltage, high current IGBT test rig was set up based on the circuit shown in Fig. 2. The DIM800NSM33-F was tested at 1800V and a 800A single current pulse in order to characterize $V_{GE(pre-th)}$ at different temperatures. A temperature controlled heat sink was used to alter the IGBT power module's T_c . The heat sink has two independent controllable heat plates allowing to heat half of the chips of the power module at one temperature and the other half at a different temperature. $V_{GE(pre-th)}$ was measured by oscilloscope and the IGBT baseplate temperatures were measured with thermocouples as references. The thermocouples are Type K Stainless Steel Washer probes with a tolerance of $\pm 1.5^\circ\text{C}$ [17]. In order to average out thermocouple errors, six thermocouples were utilized. Each thermocouple was placed in the middle between the six IGBT module mounting holes on the baseplate. A small groove was milled in the middle of the baseplate to avoid heat transfer between both heat plates when operating the heat plates at different temperatures. Different temperature settings have been used for the heat plate and after a temperature settling time the IGBT power module was turned on. A settling time is required to fulfil $T_{vj}=T_c$. Fig. 4. shows seven measurements. Five measurements where both heatsinks have the same temperature (red circle) and two measurements where half of the IGBT module baseplate (8 IGBT chips) was maintained at 20°C while the other half (8 IGBT chips) was at 80°C and 100°C respectively (blue star).

Fig. 4 shows a nearly linear relationship between $V_{GE(pre-th)}$ and T_{vj} . The sensitivity is $-2.2\text{mV}/^\circ\text{C}$. The sensitivity can be compared to $V_{GE(th)}$ and $V_{GE(miller)}$ which are $-8\text{mV}/^\circ\text{C}$ [12] and $-3\text{mV}/^\circ\text{C}$ [10] respectively. However, this comparison is indicative as both references used different power modules. All three TSEPs show linearity over a temperature range between 20°C and 125°C . The heat plates used for the characterization were unable to keep a constant temperature at 125°C . Thus linearity is indicated for values above 100°C in Fig. 4 as a dashed line. Fig. 4 shows also results from operating the IGBT power module at two different temperatures. Fig. 4 shows that in both cases ($100^\circ\text{C}/20^\circ\text{C}$ and $80^\circ\text{C}/20^\circ\text{C}$) $V_{GE(pre-th)}$ is tracking

the higher temperature. Thus one can conclude that $V_{GE(pre-th)}$ tracks the semiconductor chips with the highest temperature.

Fig. 4. Temperature variation of $V_{GE(pre-th)}$: Circles - measured voltages, Solid line - linear interpolated between measured voltages, Star - measured voltages at different heat plates temperatures.

V. IMPLEMENTATION OF $V_{GE(pre-th)}$ MONITORING CIRCUIT

The photograph of the test rig is shown in Fig. 5

Fig. 5. Photograph of the experimental set-up.

Fig. 6. Schematic of the $V_{GE(pre-th)}$ measurement for IGBT T_{vj} monitoring.

Fig. 6 shows the schematic of the IGBT T_{vj} monitoring circuit using a digital counter which is easier to implement in PIC18F24K22 hardware compared to an analogue counter. The gate driver used in this experiment is the 2BB0535T-33 board from CONCEPT [18]. This is an isolated gate driver board which is typically used for high voltage applications. If a non-isolated gate driver board is used (i.e. low voltage applications), the PWM signal which triggers the start of the counter can be directly connected to the programmable interrupt controller (PIC). For isolated gate driver circuits, as used in this experiment, the introduction of an additional isolation path between the PWM signal and the input of the PIC would be expensive. In order to avoid this, a voltage edge detector was implemented in this experiment as shown in Fig. 6. The edge detector is implemented at the gate side of the gate driver circuit and it triggers the counter once V_{GE} reaches $-8V$. In the experiment a delay time of $1.18\mu s$ was set. This is the best point of measurement just before $V_{GE(th)}$. This point was found by using initial tests using data from the oscilloscope. Once the digital counter completes the counting it activates the embedded PIC ADC to read the actual gate emitter voltage $V_{GE(pre-th)}$, and the value is transferred to the host computer.

To improve precision of the fixed delay, the PIC used has a high clock speed, 64MHz, and this can be further increased using external clock. To minimize influence of the gate resistor on drifting of the fixed delay, the gate resistor used is a Thick Film Surface Mount Resistor 1206 which is a low temperature tolerance resistor. As an alternative to a fixed time delay, it is also possible to generate an adaptive delay by measuring the gate resistor temperature in order to offset any error. This, however, will increase hardware complexity.

Table II shows results using the measurement circuit while Fig. 7 presents the results measured from the oscilloscope. $V_{GE(pre-th)}$ was measured at $t = 1.18\mu s$ (see the zoomed area in Fig 7) and based on Fig. 4, the temperatures in Table II were calculated. Table II shows that the monitoring circuit has an error of $3^\circ C$. The error is due to the resolution of ADC used being limited to 10-bit. This can be improved by using an ADC with a higher resolution. The error is also due to the linear interpolation in Fig. 4.

Fig. 7. Experimental results of the proposed $V_{GE(pre-th)}$ TSEP.

Thermo-couple ($^\circ C$)	$V_{GE(pre-th)}$ Circuit ($^\circ C$)	Error ($^\circ C$)
20	23	+3
50	48	-2
80	77	-3

VI. DISCUSSION

This section investigates the impact on environmental changes like temperature change in R_{Gext} or changes in the supply voltage V_{GG} . In addition measurement is repeated using a second power module from the same batch to show repeatability of $V_{GE(pre-th)}$ using fixed time delay.

Fig. 8. V_{GE} as a function of change in R_{Gext} caused by temperature.

Fig. 8 shows simulation results of the voltage change for an $80^\circ C$ temperature rise in R_{Gext} . The resistor has a TCR of 100ppm/K [19] thus the overall resistance changes to 3.93Ohm. Fig. 8 shows that the voltage error can be neglected as the impact on the gate emitter voltage is small.

Fig. 9. V_{GE} as a function of change in V_{GG} .

Fig. 9 shows simulation results by varying the gate supply voltage from -10V to -9.8V. The gate driver used is the 2SC0535T2A1-33 from CONCEPT [20] which comes with temperature compensation. -9.8V is an error of 2% which is within the specification. Fig. 9 shows that the time shift can be ignored that is caused by the change of the supply voltage. Fig. 10 shows the measurement on a second power module taken from the same batch to compare the measurement error between different devices.

Fig. 10. Experimental results of the proposed $V_{GE(pre-th)}$ TSEP on a 2nd power module.

At 1.18 μ s the recorded error is: 1.1% at 20°C, 0.5% at 50°C and 2.9% at 80°C. The errors show that the technique is repeatable. However if high accuracy is required, each IGBT power module must be individually characterized.

VII. CONCLUSION

This letter has presented $V_{GE(pre-th)}$ as a TSEP that requires no complex hardware, does not involve data processing and requires no current sensors. Consequently hardware requirement is low compared to other TSEPs. In addition $V_{GE(pre-th)}$ avoids self-heating which most TSEPs suffer from. $V_{GE(pre-th)}$ is measured just prior $V_{GE(th)}$ by using a voltage sensor and a counter. The letter characterizes $V_{GE(pre-th)}$ both in simulation and experimentally. The letter also shows the practical implementation of a monitoring circuit. In the characterization a 3.3kV, 800A IGBT module was used. The temperature sensitivity measured during the experiments is linear with -2.2mV/°C. It was demonstrated that $V_{GE(pre-th)}$ captures the hottest chip temperatures. The impact on external tolerances such as external gate resistor changes have been discussed. The counter could be made adaptive to compensate for possible changes. The developed monitoring circuit has a 10-bit resolution resulting in a 3°C temperature error. The error can be reduced by increasing the ADC resolution. Future work will be to demonstrate the representativeness and the performance of $V_{GE(pre-th)}$ in an operative converter configuration.

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