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Increased Mobility in Enhancement Mode 4H-SiC MOSFET Using a Thin SiO₂ / Al₂O₃ Gate Stack

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Abstract— A field effect mobility of 125 cm²/V·s and a subthreshold slope of 130 mV/dec were obtained in enhancement mode 4H-SiC MOSFETs with a channel length of 2 μm. The fabricated devices utilised a gate stack comprising a 0.7 nm thin thermal SiO₂, thereby reducing defects following oxidation, and a 40 nm thick Al₂O₃ formed by atomic layer deposition. A high mobility was maintained over a wide gate voltage range and resulted in increases of up to 120x in drain current for the same gate overdrive voltage compared to MOSFETs having a thicker thermal SiO₂ gate stack with the same effective oxide thickness fabricated alongside. Nitridation is not included in either MOSFET process.

Index Terms—4H-SiC MOSFET, channel mobility, interface traps, SiC/SiO₂

I. INTRODUCTION

As a wide bandgap semiconductor, Silicon Carbide (SiC) could yield many desirable properties in Metal Oxide Semiconductor Field Effect Transistor (MOSFET) technology, offering significant advantages over Silicon (Si) MOSFETs, particularly for applications in power electronics [1] and electronics for harsh environments [2]. But high quality oxide-semiconductor interfaces have been a major challenge in the fabrication of SiC MOSFETs. By contrast, the excellent interface formed between Si and Silicon Dioxide (SiO₂) has led to the success of CMOS technology and even in the era of high-k dielectrics an interfacial SiO₂ layer is introduced to improve the Si interface quality [3]. In SiC MOSFETs, electrically active defects close to the SiC/oxide interface have led to poor electron mobilities, typically below 10 cm²/V·s [4],[5]. Usually a gate oxide is fabricated by high temperature

oxidation of SiC in dry Oxygen [6]. This produces a range of defects such as residual Carbon (C), dangling bonds and complex C clusters that are difficult to eradicate [7],[8]. Oxide nitridation using post-oxidation annealing (POA) is commonly used to mitigate these defects, but this is only partially successful, leading to mobilities in the range of 30 - 40 cm²/V·s [4],[5]. An alternative approach has been to use a deposited high-k dielectric such as Al₂O₃ to replace the thermally grown SiO₂. Hatayama *et al* [9] claimed field effect mobilities as high as 300 cm²/V·s in SiC MOSFETs utilising a SiO₂ interfacial layer between SiC and a deposited Al₂O₃ dielectric. They concluded that an interfacial oxide layer with thickness above 2 nm degrades the interface and channel mobility. Lichtenwalner *et al* [10] obtained field effect mobilities as high as 106 cm²/V·s using a 25 nm Al₂O₃ layer formed by Atomic Layer Deposition (ALD). The interface state defect density (D_{it}) was controlled by high temperature annealing in nitric oxide (NO) prior to Al₂O₃ deposition. This had the consequence of forming an interfacial oxide of thickness 1 – 2 nm. But in both of these cases [9]-[10] the high peak mobility drops to less than 50% of its maximum value when the gate-source voltage (V_{GS}) is increased by 1 V, which will compromise device performance. Zheng *et al* [11] have recently used borosilicate glass (BSG) as a gate dielectric, obtaining a peak field-effect mobility of 180 cm²/V·s when BSG is combined with Antimony (Sb) counter-doping in the channel, but mobility again degrades rapidly with increasing V_{GS}.

Here we report SiC MOSFETs having a peak field effect mobility of 125 cm²/V·s, which degrades less severely than the previously reported high mobility SiC MOSFETs mentioned above [9]–[11]. Therefore its impact on device performance is improved, leading to drain current enhancements of up to 120× compared with control devices (fabricated using an oxidation anneal at 1150 °C). By using an oxidation anneal that is low temperature (600 °C) and for a short time (3 min), the resulting interfacial oxide layer thickness is 0.7 nm, thereby limiting the formation of defects in SiC. Shen and Pantelides [8] proposed the formation of immobile carbon di-interstitial defects (C_i)₂ in SiC as a result of thermal oxidation. Defects of this kind would go some way in explaining the poor channel mobility observed in SiC

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MOSFETs even following POA. Mobility will also be degraded by remote Coulombic scattering, which is a particular issue for deposited dielectrics such as Al_2O_3 [3]. By carrying out a post-deposition anneal of our deposited Al_2O_3 dielectric, remote Coulombic scattering is reduced. Charged defects also have a deleterious effect on the sub-threshold slope (S) [12]. Where reported [11], S can be more than $10\times$ larger than the ideal value of 60 mV/dec for long channel ($> 100 \mu\text{m}$) SiC MOSFETs, indicating high levels of charged defects even when peak mobility is high. We observe $S = 130$ mV/dec for a $2 \mu\text{m}$ gate length SiC MOSFET, consistent with reduced levels of charged defects.

II. EXPERIMENTAL

The p-type MOS capacitors and n-channel planar MOSFETs were fabricated on epitaxial 4H-SiC wafers supplied by Cree (3.84° off-axis, Si-face, n^+ (sub)/ p^+ (10^{17} cm^{-3} , $5 \mu\text{m}$)/ p^- ($5.3 \times 10^{15} \text{ cm}^{-3}$, $1 \mu\text{m}$). After standard organic, Piranha and RCA cleaning, the source and drain regions were formed by multi-energy nitrogen ion implantation to form a box doping profile ($4.7 \times 10^{19} \text{ cm}^{-3}$, 100 nm). The implantation was performed at room temperature with ion beam perpendicular to the surface and through a 30 nm thick Aluminum (Al) layer deposited on the samples. After an implantation mask and Al layer removal, a graphite capping layer [13] was used to protect the samples during activation annealing at 1700°C for 10 min . To minimize any possible SiC surface oxidation, the protective layer was then removed by cleaning in a Tegal PLASMOD 100 W Tabletop Plasma Reactor at room temperature for 90 minutes , followed by another RCA cleaning. After that, the source and drain contacts were formed by e-beam evaporation of 5 nm thick Ti and 90 nm thick Ni, followed by annealing in vacuum at 1000°C for 3 min . To protect the metal from being oxidised, 100 nm of Si_3N_4 was deposited by Plasma Enhanced Chemical Vapour Deposition (PECVD) [14]. The deposited Si_3N_4 was removed by BHF in the channel region and immediately a thin SiO_2 layer was grown at 600°C for 3 min by Rapid Thermal Processing (RTP) in a dry oxygen ambient. This was immediately followed with around 40 nm of Al_2O_3 grown by ALD to achieve an effective oxide thickness (EOT) of 29 nm for the gate stack. Adduct-grade trimethylaluminium (TMA) and H_2O were used as precursors and transported to the reaction chamber by vapor draw with N_2 carrier gas. Deposition was performed at 200°C , at a chamber pressure of 600 mTorr , with pulse/purge lengths of $0.1/4 \text{ s}$ and $0.1/6 \text{ s}$ for TMA and H_2O respectively. Then, after Al_2O_3 and Si_3N_4 layers were

etched to open source and drain contacts, the contacts were enhanced by e-beam deposition of 5 nm Ti and 150 nm Al. The devices were completed with the deposition of 150 nm Al to form the gate contacts and post deposition annealing in nitrogen ambient at 300°C for 60 min . The fabricated MOSFETs have a channel length (L) of $2 \mu\text{m}$ and a width (W) of $100 \mu\text{m}$.

Alongside fabrication of the “thin- SiO_2 ” devices just described, “thick- SiO_2 ” control MOSFETs were fabricated having a conventional high temperature oxidation. The gate oxide was grown in a dry O_2 ambient at 1150°C for 180 min , resulting in a 29 nm thick SiO_2 layer. In all other respects the thin- SiO_2 and thick- SiO_2 processes were the same. In addition to these MOSFETs, MOS capacitors were also fabricated using both the thin- SiO_2 process and the thick- SiO_2 process. The n-type MOS capacitors were fabricated on epitaxial 4H-SiC wafers supplied by Cree (7.83° off-axis, Si-face, n^+ (sub)/ n^+ (10^{18} cm^{-3} , $1 \mu\text{m}$)/ n^- ($8.72 \times 10^{14} \text{ cm}^{-3}$, $45 \mu\text{m}$)).

The thickness of the SiO_2 was estimated by using an Angle Resolved X-Ray Photoelectron Spectroscopy Theta Probe with Al $K\alpha$ source. A binding energy of 102.9 eV is observed, corresponding to a SiO_2 peak, and the SiO_2 layer thickness was estimated by areal ratio [15]. Electrical measurements were performed using an Agilent B1500A semiconductor device parameter analyzer. The density of interface traps (D_{it}) for the MOS capacitors was extracted by using the high-low method (1 MHz for high and quasi-static C-V for low frequency) [16]. The field effect mobility, μ_{FE} was determined by:

$$\mu_{FE} = \frac{L \cdot g_m^i}{W \cdot C_{ox} \cdot V_{DS}} \quad (1)$$

where g_m^i is the intrinsic transconductance [17], V_{DS} is the source-drain voltage and C_{ox} is the oxide capacitance per unit area of MOSFETs measured using split C-V configuration.

III. RESULTS AND DISCUSSION

The MOSFETs fabricated with 0.7 nm oxide (thin- SiO_2) demonstrated the highest peak mobility. Fig. 1a shows the drain current (I_D) versus the gate overdrive voltage ($V_{GS} - V_{th}$) measured at room temperature and $V_{DS} = 100 \text{ mV}$, for MOSFETs fabricated with either the thick- SiO_2 or the thin- SiO_2 process. The threshold voltage (V_{th}) is taken to be V_{GS} when $I_D = 10^{-10} \text{ A}/\mu\text{m}$. Values of subthreshold slope, S , were extracted from plots of I_D vs V_{GS} in the subthreshold region where $10^{-11} > I_D > 10^{-12} \text{ A}/\mu\text{m}$. For the devices having a thick-

Fig. 1. (a) Transfer characteristic I_D vs $(V_{GS} - V_{th})$ and (b) Output characteristic I_D vs V_{DS} for thin- SiO_2 and thick- SiO_2 .

Fig. 2. (a) I_D ratio of thin- SiO_2 / thick- SiO_2 as a function of gate overdrive: (b) impact of annealing on I_D vs V_{GS} hysteresis for thin- SiO_2 .

SiO₂ gate oxide, $V_{th} = 4.9$ V, along with a large value for $S = 550$ mV/dec. But using the thin-SiO₂ gate oxide $S = 130$ mV/dec, which indicates a lower density of charged defects in the vicinity of the channel, while the MOSFET remains enhancement mode with $V_{th} = 2$ V. Fig. 1b shows the corresponding I_D vs V_{DS} relationships for the same devices. The family of curves with increasing $V_{GS} - V_{th}$ for the thin-SiO₂ devices are indicative of good electrostatic control. Fig. 1b also includes a single $I_D - V_{DS}$ curve for a thick-SiO₂ device, where $V_{GS} - V_{th} = 5$ V. This illustrates the difference in current carrying capability for thick-SiO₂ and thin-SiO₂ devices. There is a major improvement in drain current for the thin-SiO₂ MOSFETs compared with thick-SiO₂ MOSFETs, for the equivalent gate overdrive voltage ($V_{GS} - V_{th}$). This is further clarified in Fig. 2a, which is a plot of the ratio $I_D(\text{thin-SiO}_2) / I_D(\text{thick-SiO}_2)$ as a function of $V_{GS} - V_{th}$. This current ratio peaks at 120 for a gate overdrive voltage of 1.7 V, while at 5 V the current ratio is 35.

A previously recognised concern relating to the use of a high-k dielectric such as Al₂O₃ in the gate stack is the hysteresis in I_D vs V_{GS} , which arises through trapping and de-trapping of electrons in the oxide as the gate voltage is swept [3]. Oxygen (O) vacancies have 5 stable charge states in the Al₂O₃ energy band gap. The change in oxide trapped charge leads to a threshold voltage shift corresponding with the hysteresis observed in Fig. 2b. The effect can be reduced following densification of the deposited Al₂O₃ layer by a low temperature anneal. Temperatures in the range 150 °C to 400 °C were investigated to optimise this anneal. The reduction in voltage hysteresis is shown in Fig. 2b, changing from 4 V for the as deposited Al₂O₃ film to 0.7 V following an anneal at 300 °C for 60 min. In addition to reducing the hysteresis, the electron mobility is found to increase, corresponding with a reduction in remote Coulombic scattering from charges in the dielectric. The residual hysteresis in I_D vs V_{GS} following the 300 °C anneal, although much reduced, is larger than that found in MOSFETs fabricated using the thick-SiO₂ process, which is 0.2 V. This indicates that the mobility obtained remains compromised by some outstanding coulombic scattering from Al₂O₃, suggesting that further improvement in reduced hysteresis and increased mobility may be possible.

Fig. 3. (a) μ_{FE} and corresponding I_D of fabricated MOSFETs as a function of gate overdrive and E_{eff} in SiC; (b) Distribution of D_{it} near valence and conduction band edges.

High electron mobility is obtained for SiC MOSFETs fabricated with the thin-SiO₂ process. Fig. 3a is a plot of field

effect mobility versus effective electric field in the SiC, close to the oxide interface, E_{eff} . Since E_{eff} is a function of V_{GS} , the gate overdrive voltage is also indicated on the same graph. It can be seen that the mobility peaks at 125 cm²/V·s for a gate overdrive of 4 V and an effective electric field, E_{eff} , of 0.35 MV/cm. Mobility remains above 120 cm²/V·s up to a gate overdrive of 6 V, corresponding to an effective electric field in the SiC of 0.49 MV/cm and an effective electric field in the gate dielectric of 2.2 MV/cm [11],[18]. For higher E_{eff} the mobility will decrease, but only drops by 25% of its peak value for a gate overdrive of 8 V, corresponding to $E_{eff} = 0.6$ MV/cm and an effective electric field in the gate dielectric as high as 3 MV/cm.

The mobility in the thin-SiO₂ device is much higher than in the thick-SiO₂ (control) device, where the peak mobility is only 7 cm²/V·s, corresponding to an enhancement factor of 18x in peak mobility using thin-SiO₂. Fig. 3a represents our best measured mobility, but high mobilities were obtained in all working devices using the thin-SiO₂ process, with many in excess of 100 cm²/V·s.

Fig. 3b shows the density of interface traps (D_{it}) as a function of energy in relation to the valence band maximum ($E - E_v$) for the entire band gap, obtained from both p-type (valence band edge) and n-type (conduction band edge) MOS capacitors. D_{it} levels in the range from 6×10^{11} - 5×10^{10} cm⁻²eV⁻¹ were found when the thin-SiO₂ process was used to fabricate MOS capacitors. This represents a reduction in D_{it} by 1-2 orders of magnitude compared to MOS capacitors fabricated with the thick-SiO₂ process. Furthermore, the MOS gate stack comprising the thin-SiO₂ was able to withstand electric fields of 6.5 MV/cm with a leakage current density around 1×10^{-6} A/cm², thereby demonstrating that this gate oxide stack is robust.

IV. CONCLUSION

We have demonstrated a way to increase the channel mobility of enhancement mode SiC MOSFETs, explicitly by using a thin-SiO₂ process comprising 0.7 nm thin SiO₂ layer and Al₂O₃ deposited by ALD to achieve an EOT of 29 nm. MOSFETs fabricated with the same EOT using a thick SiO₂ layer were fabricated alongside for comparison, but nitridation was not included in either process. The quality of the SiC/oxide interface is improved using the thin-SiO₂ process and in particular defects, resulting from prolonged oxidation, are reduced. These results are consistent with a reduction in C related defects, which has been proposed previously [8]. A peak channel mobility of 125 cm²/V·s is recorded, together with a subthreshold slope of 130 mV/dec and D_{it} levels in the range from 6×10^{11} - 5×10^{10} cm⁻²eV⁻¹, that further indicates good control of charged defects in the SiC. Remote Coulombic scattering from charge in the Al₂O₃ deposited dielectric is mitigated by a 300 °C anneal, which also reduces the hysteresis in V_{th} from 4 V to an acceptable 0.7 V, but remains a future challenge. This novel process approach is highly applicable to SiC power MOSFETs.

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