Mitigation of DC Current Injection in Transformer-less Grid Connected Inverters Using a Voltage Filtering DC Extraction Approach

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Abstract — Transformer-less grid connected PV inverters are an attractive technology choice due to their high-efficiency performance and relatively small volume. However, in the absence of galvanic isolation, dc current can potentially flow into the grid and adversely affect the grid performance. In addition, as the sinusoidal ac output is significantly larger than the dc injection component, accurate dc current sensing at the inverter output remains a technical challenge. As a result, this paper proposes a two-stage dc voltage detection technique that employs an isolated RC attenuation circuit and a software dc-component filtering algorithm. The principle of the proposed technique can be applied in many switch mode power converter topologies. The simple and cost-effective combination facilitates dc component extraction within the accuracy of 1 mV, moreover, this can be further used as digital dc feedback for active current control purposes. Experimental results from a laboratory prototype demonstrate the high performance of the proposed dc extraction and suppression approach.

Keywords—Transformer-less, Grid Connected, Power Quality, DC Extraction, DC Injection Suppression.

I. INTRODUCTION

PV inverter technology is primarily driven by cost, efficiency and reliability. For this reason, a diverse range of grid connected PV inverter topologies and control methods have been developed and researched in industry and academia. Among these innovative topologies, transformer-less grid connected inverters have drawn increasing attention in low-power PV applications [1, 2]. Compared to alternative inverter systems which typically insert a bulky transformer between the PV panel and the utility grid, transformer-less topologies generally offer improved efficiency with lower cost and volume [2-6]. However, the lack of galvanic isolation has technical and safety implications. Among these implications, dc current injection into the grid continues to be a major technical challenge.

DC current injection may arise due to several reasons, including; non-ideal semiconductor switching characteristics,

such as subtle differences in on-state resistance and voltage drops, asymmetries in switching behaviors and gate drive circuit delays, small dc bias in the current reference or errors within the digital controller, and non-linearity and offset drift in the current transducer [7],[8]. Although dc current injection from an individual inverter may be small, the accumulative effect from multiple grid connected inverter units can potentially saturate the distribution transformer, affect the normal load operation and degrade power cables over time [7]. As a result, strict guidelines and recommendations are imposed to limit the dc injection from individual inverter units [9],[10]. However, it has been found that even a small dc bias can perturb the operation of the distribution transformer, introducing undesirable currents which accumulatively result in additional losses and overheating problems [11]. For this reason, recent studies have looked to address the issue of dc current injection into the grid via a range of hardware and software solutions.

One hardware solution is to use a series capacitor in the output filter stage to block the dc current flowing into the grid. This normally requires a bulky and expensive capacitor to minimize its impact on the output current. Polarized electrolytic capacitors are not a desirable choice given the ac output of the inverter, however, they provide the necessary high capacitance value and voltage ratings [12]. As a result, a polarity protection circuit is often included to preserve the integrity of the capacitors. An alternative solution is proposed in [8], where the offset drift and nonlinearity of the current control sensor is actively calibrated. However, the calibration process requires double the sampling frequency, and it is only effective for specific converter topologies. Recently, attention has focused on high resolution dc measurement and control techniques. Combined with dedicated control schemes, the dc current injection can be actively compensated using an additional suppression loop. A diverse range of dc detection schemes has been investigated in the literature. The authors in [13] introduce a direct dc measurement technique based on a simple magnetic circuit composed of a magnetic core and compensation winding to overcome the challenge of large ac/dc component ratios. However, the performance of the dc measurement relies greatly on the quality of the compensation winding. Furthermore, accurate dc current determination from the combined flux measurements is a non-trivial task. A more recent research is proposed in [14], where a 1:1 coupled inductor combined with a small-range current sensor is applied to measure dc current components. However, this technique requires an additional sensor set combined with a specially designed coupled-inductor to achieve robust performance.

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Alternative studies have discussed dc voltage sensing techniques. Authors in [15] investigate a solution using a small 1:1 voltage transformer and an RC circuit to detect the dc offset voltage. However, complete removal of the dominant ac voltage component is difficult considering the phase shift between the grid voltage and the inverter output; hence high accuracy dc voltage measurements are challenging. As a result, in [16], a double-stage RC circuit connected across the ripple filter is introduced. However, the detected dc voltage offset, which is very small, is prone to corruption from noise. In addition, there are high common-mode voltage problems to consider. For this reason, a novel dc suppression method is proposed in [17],[18]. Here, the dc voltage offset is measured at the inverter output via a differential amplifier and a low-pass filter. Whilst the scheme is more robust against noise, accurate extraction of the dc component is challenging due to the large full-scale range of the inverter output signal. Other state-of-the-art dc sensing solutions have been investigated using non-linear reactors [11], [19], [20]. Typically, these schemes offer precision sensing but are very sensitive to the reactor design, and rely on sophisticated control solutions.

In contrast to the aforementioned measurement techniques, there are several active software solutions that attempt to achieve dc component measurements from existing voltage and current measurement signals. Generally, a major advantage is eliminating the need for additional hardware. In [21], a virtual capacitor concept is proposed, where the feedback loop acts equivalently as a series blocking capacitor from control aspect; whereas the major concern of the virtual capacitor approach is the accuracy of the current sensing circuit. If the sensor operating point drifts or the dc injection is not correctly sensed, the feedback control is likely to offer poor performance. The authors in [22] introduce an indirect dc estimation based on the software extraction of the dc link line-frequency voltage. As the dc link capacitor voltage is already sensed within the inverter system, no extra hardware is needed. However, owing to the minimal line-frequency voltage ripple on the dc link capacitor, accurate measurement of this ripple component from a much larger dc voltage can be challenging and any inaccuracy in the measurement ultimately results in degraded dc mitigation performance. In summary, whilst many methods are proposed in the literature, it is clear that technical challenges still exist with sensing and controlling dc current injection in grid-connected PV systems.

For this reason, in this paper, a novel two-stage dc voltage detection technique is proposed to mitigate the dc component in grid-connected inverter systems. The scheme employs an RC filter attenuation circuit and a software dc-component extraction algorithm. This combination facilitates very accurate dc component extraction, with minimal hardware requirements. This dc output signal is then used as a dc feedback signal for current control purposes. Unlike many solutions, it is not generally dependent on the power electronic converter topology. Hence, it is a desirable solution for dc current compensation in most grid connected inverter systems.

II. PROPOSED DC VOLTAGE DETECTION

Typically, the single-phase inverter output is a 380-400V PWM frequency switching waveform that is connected to the grid via a low-pass filter (LPF). Due to the aforementioned

Fig. 1. Diagram of proposed dc voltage suppression for transformer-less grid connected inverter

imperfections of the system, the PWM waveform of this inverter output also contains a minimal dc voltage offset V_{dc} (in millivolts), which originated from the dc current injection I_{dc} and parasitic resistance of the system. Put simply:

$$V_{dc} = I_{dc}(R_e + R_g) \quad (1)$$

where R_e and R_g are the values of ESR of the filter and grid respectively. Fig. 1 shows the block diagram of a typical transformer-less inverter with the proposed dc suppression method. Whilst the classic current control loop maintains the general operation of the inverter, an extra closed-loop to suppress the dc voltage offset is integrated into the feedback path. The dc detection comprises of a passive attenuation circuit directly connected to the inverter output and a digital filtering algorithm. The passive attenuation circuit reduces the ac voltage component to the nominal analog-to-digital converter (ADC) voltage input but, importantly, without suppressing the dc component. To achieve this, a low cut-off frequency is required, but this results in the dc component becoming a more significant element in the filter output. The filter output voltage is then digitized and presented to the microcontroller. With a much smaller ac/dc component ratio, the software filtering stage is implemented on the microprocessor to accurately extract the dc voltage component found in the inverter output voltage. The following sections describe the rationale and design considerations for the passive attenuation circuit and software filtering algorithm.

A. Pre-Passive Attenuation Stage

The RC low-pass filter is a simple and effective way of attenuating ac signals whilst preserving the dc component of the input signal. In previous studies, with an appropriate cut-off frequency, a traditional second-order low-pass filter (Fig. 2) is capable of achieving a small dc voltage across the second stage capacitor C_2 [16]. This is a hardware-only solution, where the ac content is not completely eliminated by the LPF, and a very low cut-off frequency is needed and consequently, bulky components. Moreover, the high common-mode voltage across the capacitor results in problems with interfacing with the digital controller hardware. A simple, low-cost voltage divider can be used to overcome this problem; however, this is not a particularly robust solution. It also adds a further stage to the

Fig. 2. Filtering based on second order passive LPF used in [16]

Fig. 3. Alternative active LPF solution used in [17]

Fig. 4. The proposed passive attenuation circuit

process, and therefore represents an additional source of potential loss of accuracy.

Alternatively, the use of an isolation amplifier with a high common-mode rejection ratio (CMRR) can resolve the problem. As shown in Fig. 3, a high-precision differential amplifier is introduced which bridges the low-pass filter and the inverter output [17]. This is still a hardware-only solution, although it does resolve the issue of common-mode voltage using the high CMRR and isolation of the differential amplifier, thus eliminating the need for an additional voltage divider stage. However, the use of the differential amplifier itself degrades accuracy itself as a result of reducing the output voltage to within the amplifier supply rails. Since the ac voltage component is attenuated in a similar fashion to the dc voltage component, the difficulty of extracting a very small dc still exists, but becomes even harder due to the much smaller voltage scales involved. This, in turn, has an impact on the overall accuracy of the results. Ideally, even with a differential amplifier, the cut-off frequency of the low-pass filter must be as low as possible to maximize ac signal attenuation. However, practical limitations have to be observed; for example, a very low cut-off frequency requires increasingly large and more expensive capacitor to be used, and significant measurement delay is introduced.

As the precision of the dc extraction is normally limited when solely based on a hardware filtering solution, the method proposed in this paper combines simple hardware and software stages to extract and eliminate the dc injection. The hardware stage is a passive attenuation circuit that scales down the inverter output voltage to the input range of the ADC of the microcontroller between 0 to 3V for the DSP used in this investigation. The circuit is directly connected to the inverter output, in which a simple first-order RC low-pass filter is

Fig. 5. Moving average filter applied to attenuated voltage output

incorporated as the attenuator. An appropriate cut-off frequency guarantees that the residual ac component falls into the ADC range, whilst fully preserving the dc component. Although this dc component is still small, the ac/dc ratio is substantially better, thus improving the sensitivity. Fig. 4 shows a simplified schematic diagram of the passive attenuation circuit. The attenuated voltage is accurately sensed by the instrumental amplifiers. As the accurate detection of the minimal dc components may still be technically challenging, a secondary filtering stage is proposed to overcome this issue. Once the voltage measurement is sampled and digitized by the microprocessor, the extraction can be carried out based on a digital signal processing technique. It is worth mentioning that an isolation amplifier is included in the passive attenuation circuit. This provides electrical isolation and a safety barrier between the analogue measurement and digital input. Although such a device potentially increases the cost of the overall circuit, the weight and size of the system are greatly reduced compared with implementing of a bulky line-frequency transformer. Most importantly, with a higher power rating, the price of isolation will stay fixed while the cost of mains transformers are significantly rising.

The use of the RC filter is 1st order, and it has higher cut-off frequency compared to [16] and hence smaller size and lower cost. Moreover, the dc/ac ratio is much higher than [17] as there is no attenuation of the dc component. By adding the software filtering the proposed method will outperform those in prior research.

B. Post-Digital Filtering Stage

Once the output of the passive attenuation circuit has been sampled by the system microprocessor, the residual ac component is passed through a digital signal processing technique that is used to extract the dc component. The advantages of applying a secondary digital filtering stage are that, firstly, it offers a very flexible solution. The type and tuning of the filter can be modified in software, and it can be readily adjusted until an optimal solution is achieved. Secondly, it can alleviate some of the demanding very low cut-off frequency requirements of the passive filter; thus some of the burdens can be taken up by the digital filter stage. For the purpose of dc component extraction, the remaining periodic ac quantities from the attenuation circuit are removed using an integration and averaging process. This can be mathematically presented as follow.

The output voltage from the attenuation circuit comprises of both ac and dc components:

$$V_c(t) = V_{ac}(t) + V_{dc} = V_{AC} \sin(\omega t + \varphi) + V_{dc} \quad (2)$$

Fig. 6. Control diagram of dc voltage suppression

Ideally, over one mains frequency period (T), the integral of the ac voltage $V_{ac}(t)$ is zero. For a continuous system, this can be expressed as a sliding window integration in (3).

$$A_1(t) = \frac{1}{T} \int_{t-T}^t V_{ac}(\tau) dt = 0 \quad (3)$$

Therefore, the dc component can be determined by simply averaging the integral output.

$$A_2(t) = \frac{1}{T} \int_{t-T}^t V_c(\tau) d\tau = \frac{1}{T} \int_{t-T}^t V_{dc}(\tau) d\tau = V_{dc} \quad (4)$$

From (2) to (4), the implementation of periodic integral averaging (once per mains cycle) is required to extract the dc offset from the attenuated output. Due to the relatively low frequency of the mains ac voltage and the potential impact of the measurement noise, the performance of a one-off periodic integration calculation has been shown to be unsatisfactory. Therefore, a sample-based moving average filter (MAF) is applied to improve the accuracy of offset detection. Assuming N samples are taken over a given mains cycle, the periodic integral can be updated as each new sample arrives. As such, a rolling average over the last 360° of mains frequency is obtained, which effectively produces a real-time update on the dc component, as shown in Fig. 5. Mathematically, this can be expressed as:

$$A(k) = \frac{1}{N} \sum_{k_M - (N-1)}^{k_M} [V_{ac}(k) + V_{dc}(k)] = V_{dc} \quad (5)$$

In (5), $V_c(k_M)$ is the current sample at the output of the attenuation circuit, and $M \geq N - 1$. Initially, an average of the first N samples from $V_c(k_{M-(N-1)})$ to $V_c(k_M)$ is calculated to derive the dc component present in the sampled signal. In the next discrete step, the average is taken from $V_c(k_{M+2-N})$ to $V_c(k_{M+1})$, and this iterative process continues so long as the system is operational. Since the average calculation is repeated at each sampling point, the impact of noise is greatly suppressed and the robustness of the dc voltage offset detection is guaranteed. The fundamental frequency of the attenuated output is the same as the grid frequency, f_g , which in the UK is 50 Hz. Thus, the window frequency of the MAF is set to 50 Hz as well to provide the attenuation of the ac signal. Assuming that the microprocessor ADC channel has a sampling frequency f_s , of 20k Hz, then the number of samples acquired over one mains period N can be calculated as:

$$N = \frac{f_s}{f_a} = 400 \quad (6)$$

Therefore, in order to achieve dc offset voltage in this case, the MAF calculates the rolling average of the latest 400 samples.

Fig. 7. Frequency response of dc extraction

$$V_{dc} = \frac{1}{400} \sum_{k_{M-399}}^{k_M} V_c(k) \quad (7)$$

It is worth mentioning that the window frequency of the MAF is synchronized to the grid voltage via the system phase lock loop (PLL), as shown in Fig.1, thus any deviation in grid frequency can be taken into account. In other words, the number of samples N is adaptive with respect to the real time measured grid frequency.

By comparing the dc offset voltage with the dc voltage demand which is typically set to zero, the dc error is regulated via adding the compensation current from dc controller to the current reference. Consequently, with proposed accurate dc extraction, the dc suppression loop can robustly remove any dc voltage offset in the system, therefore compensating for the dc current injection.

III. DC EXTRACTION SENSITIVITY AND FREQUENCY ANALYSIS

A. Analysis of Proposed DC Voltage Suppression Loop

The control diagram of the dc suppression loop is shown in Fig. 6. The hardware attenuation circuit is composed of an RC attenuation circuit G_f , which has a cut-off frequency of ω_c , and a voltage measurement amplifier G_{amp} of unity gain. The transfer function of the circuit G_c can be expressed as in (8).

$$G_s(s) = G_f G_{amp} = \frac{V_c(s)}{V_{out}(s)} = \frac{\omega_c}{s + \omega_c} \quad (8)$$

By considering the sampling process in the ADC with a sample time of T_s , the z-domain representation of the attenuated output V_C can be obtained as:

$$G_{scale}(z) = \frac{V_c(z)}{V_{out}(z)} = \frac{1 - e^{-\omega_c T_s}}{z - e^{-\omega_c T_s}} \quad (9)$$

$$V_c(z) = \frac{1 - e^{-\omega_c T_s}}{z - e^{-\omega_c T_s}} V_{out}(z) \quad (10)$$

The secondary MAF is then implemented in the microprocessor to filter out the dc component. As it is an averaging process with a sliding window of N samples V_c (at line frequency), a mathematical representation in the z -domain can be derived in (12), based on the formula for a geometric series.

$$G_{MAF}(z) = \frac{V_{dc}(z)}{V_c(z)} = \frac{1 + z^{-1} + z^{-2} + z^{-3} + z^{-4} + \dots z^{-N+1}}{N} \\ = \frac{1 - z^{-N}}{N(1 - z^{-1})} \quad (11)$$

Thus, a z-domain transfer function of the dc extraction process can be obtained as:

$$G_{ex}(z) = \frac{V_{dc}(z)}{V_{out}(z)} = \frac{(z^N - 1)(1 - e^{-\omega_c T_s})}{N(z^N - z^{N-1})(z - e^{-\omega_c T_s})} \quad (12)$$

The inverter output voltage contains ac quantities at the integer multiple harmonics and switching frequency. Given the rolling samples $N = 400$, a sample frequency $f_s = 20 \text{ kHz}$ and the cut-off frequency $\omega_c = 1.38 \text{ rad/s}$ (0.22 Hz) of the RC attenuation filter. The frequency response of the extraction is shown in the magnitude plot in Fig. 7. With the combination of the passive RC attenuator and software MAF, increasing attenuation is observed over the frequency spectrum. The large attenuation at integer harmonics removes the redundant ac components, resulting in a precise dc measurement. This dc measurement is fed to a simple dc controller $C_{dc}(z)$, and the dc voltage offset can be completely removed via the compensation current to the current reference. Therefore, whilst the classic current control loop maintains the general operation of the inverter, the suppression loop robustly removes any dc current component.

B. Analysis of Detecting Sensitivity to Potential Errors

The sensitivity of dc detection is clearly improved with the use of the attenuation circuit and software filtering. However, the actual accuracy in terms of residual dc bias is analyzed by taking into consideration the potential errors in the operating process. Compared to current transducers, the op-amps used in the passive attenuation circuit have much better characteristics in terms of offset drift and non-linearities. Careful calibration can remove the primary offset voltage V_{os} , however, the offset voltage drifts with operating temperature. For precision op-amp, the temperature coefficient V_{Tos} lies in the range 0.1-10 $\mu\text{V}/^\circ\text{C}$. Thus, the accuracy-sensitivity to temperature S_T can be presented as:

$$S_T = \frac{V_{Tdrift}}{V_{dcs}} = \frac{V_{Tos} \Delta T}{I_{dcs}(R_e + R_g)} \quad (13)$$

where the I_{dcs} , V_{dcs} are the maximum dc current injection given in norm, and its corresponding dc voltage value. ΔT is the temperature change in during the operating condition, and the V_{Tdrift} is the voltage offset drift with temperature.

In addition, the ADC can potentially introduce errors into the software filtering stage, thus affecting the accuracy of the dc extraction. With the exception of the calibrated offset and ADC quantization errors, neither differential non-linearity (DNL) nor the integral of DNL (INL) errors can be easily corrected. In a K-bit ADC, the accuracy-sensitivity to DNL and INS errors are given as:

$$S_{DNL} = \frac{A + B}{2^K} \quad (14)$$

where A and B are the DNL and INL error in least significant bit (LSB).

Lastly, as the number of samples N in the MAF is an integer, mismatch errors are introduced by neglecting the fractional component of calculated samples in (6). As might be expected; the lower the sampling frequency, the greater the errors. The average sensitivity to the mismatch errors of MAF S_{MAF} can be represented as:

$$S_{MAF} = \frac{X}{N} \quad (15)$$

where X is the neglected fraction in integer sample number.

The overall sensitivity to potential errors S_e in the proposed dc detection process can be obtained as:

$$S_e = S_T + S_{ADC} + S_{MAF} \quad (16)$$

With the use of high resolution 12-bit ADCs and a sampling frequency of 20 kHz, S_{ADC} and S_{MAF} are minimal, and can generally be neglected. This is confirmed in (17), where the maximum ADC errors of ± 2 LSB and a maximum fraction of 0.5 are introduced. As the typical V_{Tos} and I_{dcs} are given as 0.6 $\mu\text{V}/^\circ\text{C}$ and 5 mA (readily obtained from the component datasheets and norm [9]), with an operating temperature change ΔT of 50 $^\circ\text{C}$ and parasitic resistance of 0.3 ohms, the overall sensitivity to potential errors of the dc detection system is:

$$S_e = \frac{30\mu\text{V}}{5 * 0.3 \text{ mV}} + \frac{2}{2^{12}} + \frac{0.5}{400} = 2.17\% \quad (17)$$

IV. EXPERIMENTAL VALIDATION

The experimental performance of the proposed dc voltage extraction and mitigation method is validated on a laboratory designed grid connected H-bridge inverter. The current control and dc suppression are implemented on a 32-bit, float point DSP (Texas Instruments TMS320F28377D), with 12-bit ADC. The DSP is also used for data acquisition which is achieved by a graphical user interface (GUI) developed in MATLAB. The inverter is operated with a 20 kHz unipolar PWM switching scheme from a 50 V dc link voltage. An LCL low-pass filter is connected to the inverter output to provide adequate attenuation of the high-frequency switching harmonics. Although the research focuses on the transformer-less topology, as the inverter system is connected to the utility grid, the presence of dc injection during the experiments would potentially threaten the sensitive equipment that connected to the same common coupling point. Thus, an isolation transformer is employed for protection purposes. In this way, the dc current injection still can be monitored at the inverter side, but has no impact on the grid.

To confirm the performance of the proposed dc suppression, a hardware dc measurement circuit that consists of a series resistor and a parallel external RC circuit with a cut-off frequency of 0.35 Hz, is also connected for verification purposes [8]. This is used only to verify the oscilloscope and DSP measurements of the dc injection. The voltage of the capacitor is accurately measured by a sensitive multi-meter, therefore, any existing dc injection would accordingly display on the multi-meter. A list of system parameters are presented in the Table I. Fig. 8 shows the interior layout of the laboratory inverter prototype, where the passive attenuation circuit is RC attenuator that connected to the inverter output.

Fig. 8. Internal layout of experimental inverter test-rig

TABLE I
EXPERIMENTAL PARAMETERS

Symbol	Quantity	Value (Unit)
V_{dc}	DC Link Voltage	50 (V)
V_g	Grid Voltage RMS	35 (V)
L_{in}	Inverter Side Inductor	0.6 (mH)
L_g	Grid Side Inductor	0.1 (mH)
C_f	Filter Capacitor	10 (μ F)
f_{sw}	Switching Frequency	20 (kHz)
R_s	Resistors in Attenuator	72 (kohm)
C_s	Capacitors in Attenuator	10 (μ F)
f_c	Cut-off Frequency of RC Attenuator	0.22 (Hz)

The current error in the controller can be calculated as the difference between the current reference I_{ref} and current measurement I_{gm} . With the current sensor offset I_{offset} that mimics the dc current injection [17], the expression of current error I_{error} is given as:

$$I_{error} = I_{ref} - I_{gm} = (I_{ref} - I_{offset}) - I_g \quad (18)$$

where the I_g is the injected grid current. Consequently, from (18), the existing dc injection in the simulation can be equivalently replaced with a dc onto the sinusoidal current reference.

A. Performance of Passive Attenuation Circuit

The inverter rig is operated from a 50 V dc link voltage at 20 kHz switching frequency, injecting a 5 A RMS current to the grid at unity power factor. As shown in Fig. 9, the inverter output is a switching frequency waveform, which has an alternating polarity based on the grid current. The variable duty cycles of the PWM voltage pulses show a large number of frequency components at the inverter output.

Fig. 10 shows the attenuated inverter output voltage which is dominated by the line frequency component. Since the attenuator provides a great attenuation of the frequency harmonics, but not for dc component, the residual ac voltage has an amplitude of only 0.3 V, taking into account that the RC filter is designed for the rated dc voltage. This facilitates the

Fig. 9. Inverter output current and voltage

Fig. 10. Voltage output from passive attenuation circuit

process of dc extraction as it further reduces the ratio of ac and dc components. However, owing to the features of MAF shown in Fig. 7, where an enormous attenuation is applied to the fundamental and integer harmonics, the residual ac component would hardly affect the dc extraction even with the rated dc link voltage. As mentioned before, deviation in grid frequency is compensated by synchronizing the window frequency to the mains frequency via PLL. In this investigation, no significant changes were observed in laboratory grid voltage frequency (always between 49.5 to 50.5 Hz; corresponding N from 396 to 404). However, in weak grid applications, greater variation might clearly be observed, hence the need to update N.

B. DC Detection and Suppression

By using the external measurement circuit, the dc current injection in the test rig is first measured at -65 mA without applying any dc bias to the current reference. Fig. 11 shows that dc offsets of 50 mA and 100 mA are separately injected to the current reference, according to (13), at 6.4 s and 12.8 s. The dc current injection in the test rig is respectively calculated at around -15 mA and 35 mA (50 mA and 100 mA higher than the -65 mA initial dc current). As expected, Fig. 11 shows that the dc voltage measurement follows the step change in the dc reference with a response time of 1.8s. This is confirmed with the R_s , C_s given in Table I. A significant amount of noise is revealed owing to the high scale factor of the oscilloscope. Fortunately, this is primarily introduced by the digital-to-analogue channel and measurement probes and does not actually exist in the processing signals. The accuracy of extraction is confirmed by capturing the steady-state dc voltage measurements under each condition (Section A, B, C) digitally.

Fig. 12 shows the steady-state digital dc voltage extraction of section A, B and C from the DSP, with values separately confirmed as -24 mV (± 1 mV), -6 mV and 12 mV (± 1 mV).

Fig. 11. DC voltage measurement with given dc reference

Fig. 12. DC measurement in the microprocessor

With a step change of 50 mA current in the dc reference, the responses show a step of 18 mV. From (1), the resistance of the output path can, in turn, be calculated as 0.36 ohm at the time of measurements.

Based on the results for dc voltage extraction, the levels of dc current injection under the three conditions are confirmed as -67 mA, -17 mA and 33 mA, which show good agreement with the results of the external dc measurement circuit. Since the deviation in the measurement is approximately ± 1 mV, the accuracy of dc extraction using the proposed method is validated. From this, the dc current component can be mitigated through a simple dc controller.

C. DC Suppression Performance

Initially, without injecting any dc into the current reference, the effectiveness of dc suppression is verified only taking into consideration the existing dc injection in the test rig. Fig. 13 shows the waveforms of dc voltage measurement and compensation current, where the dc injection is determined using the proposed extraction method. By enabling the suppression loop at the time point of 3.5 s, a compensation current starts to arise, which gradually causes the dc component in the system to decline. From the zoomed dynamic response, it can be clearly seen that the dc voltage measurement converges to zero with a damping response of less than 3 s. As

Fig. 13. DC voltage offset compensation

Fig. 14. DC injection measurement with/without dc suppression

Fig. 15. Harmonic distribution of nature/compensated output current

the deviation in the proposed dc detection has been proven to be within ± 1 mA, the compensation current performs with a small oscillation of 3 mA due to the existence of parasitic resistance in the output path. Despite this, the dc component is still substantially mitigated by the proposed suppression loop. Whilst the dc voltage measurement reaches zero in the steady state; the compensation current, around 60 mA, is added to the current reference, which counters the dc current in the system and assists to remove the dc current injection.

By deliberately introducing a dc into the current reference, the dc component in the sinusoidal output current is calculated separately by switching the proposed dc suppression on and off. The process is repeatedly performed for dc reference levels from 0 to 100 mA in steps of 10 mA, and the results are recorded in Fig. 14. Compared with the ramped dc injection using the conventional current control method without proposed dc suppression, the implementation of the proposed dc suppression loop effectively limits the dc of the output current within 5 mA, regardless of the changes in dc reference.

As the dc suppression is linked to the current control of the inverter system, it is important to make sure that the dc suppression loop does not affect the quality of current injected to the grid. For this reason, Fig. 15 shows the harmonic distribution between for output current and compensated output current separately via FFT analysis. The fundamental and

multi-integer harmonics show good similarity, with values of averaged total harmonic distortion (THD) at 4.73% and 4.65% respectively. This analysis confirms that the output current is free of any effect from the proposed dc suppression loop as the residual ac components are minimal compared to other dc suppression methods. Meanwhile, the dc component, which appears at a magnitude of 0.75% in the output current, has been completely removed from the compensated output current.

V. CONCLUSION

This paper investigates a novel dc suppression method for grid connected transformer-less PV inverter systems. As the accuracy of the miniscule dc extraction from a very large ac signal is challenging in previously suggested approaches, the proposed method has introduced a passive attenuation circuit and a software moving average filter. Such a combination provides a robust determination of the dc component with increased accuracy and sensitivity. The attenuation of the frequency spectrum has been demonstrated in a frequency analysis and Bode plot. Following this, dc mitigation is established via an extra dc suppression loop with a simple dc controller. By introducing a set of step-changes dc to the current reference, the experiment results demonstrate the performance of the dc measurement suppression technique under grid connected conditions. The output current is not affected by implementing the dc suppression loop. The harmonic performance shows a similar THD in the compensated output current, whilst the dc component is significantly mitigated.

In conclusion, the presented approach is low-cost, simple, and highly effective and can make a positive contribution for any grid connected PV inverter system. Unlike many other solutions presented in literature, it is not specific to any power converter topology. This makes it a very flexible method.

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